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M/B Schematics Document

AMD FP6 Cezanne H Platform with DDR4+NV GN20-E3 GPU

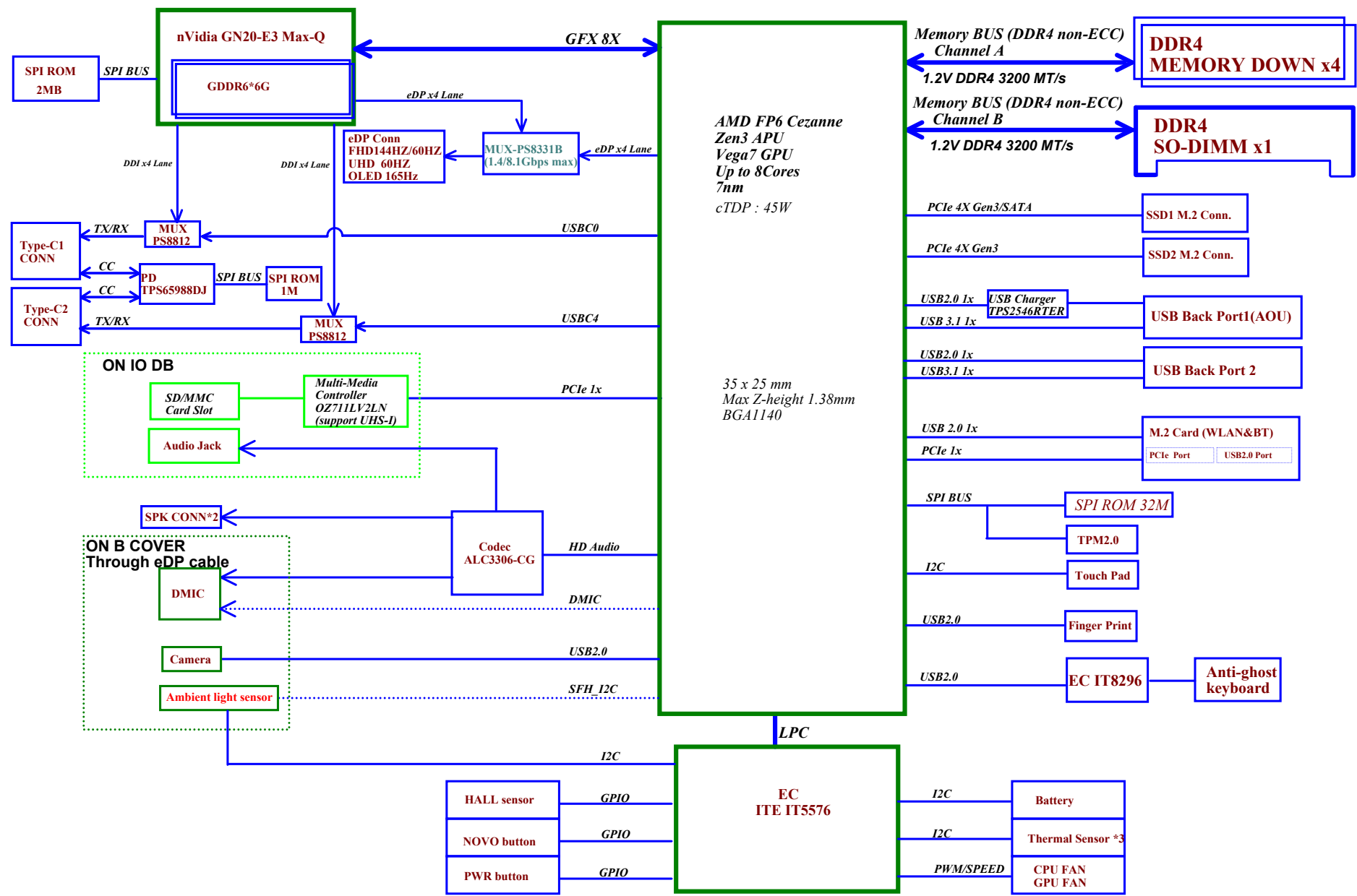
Content

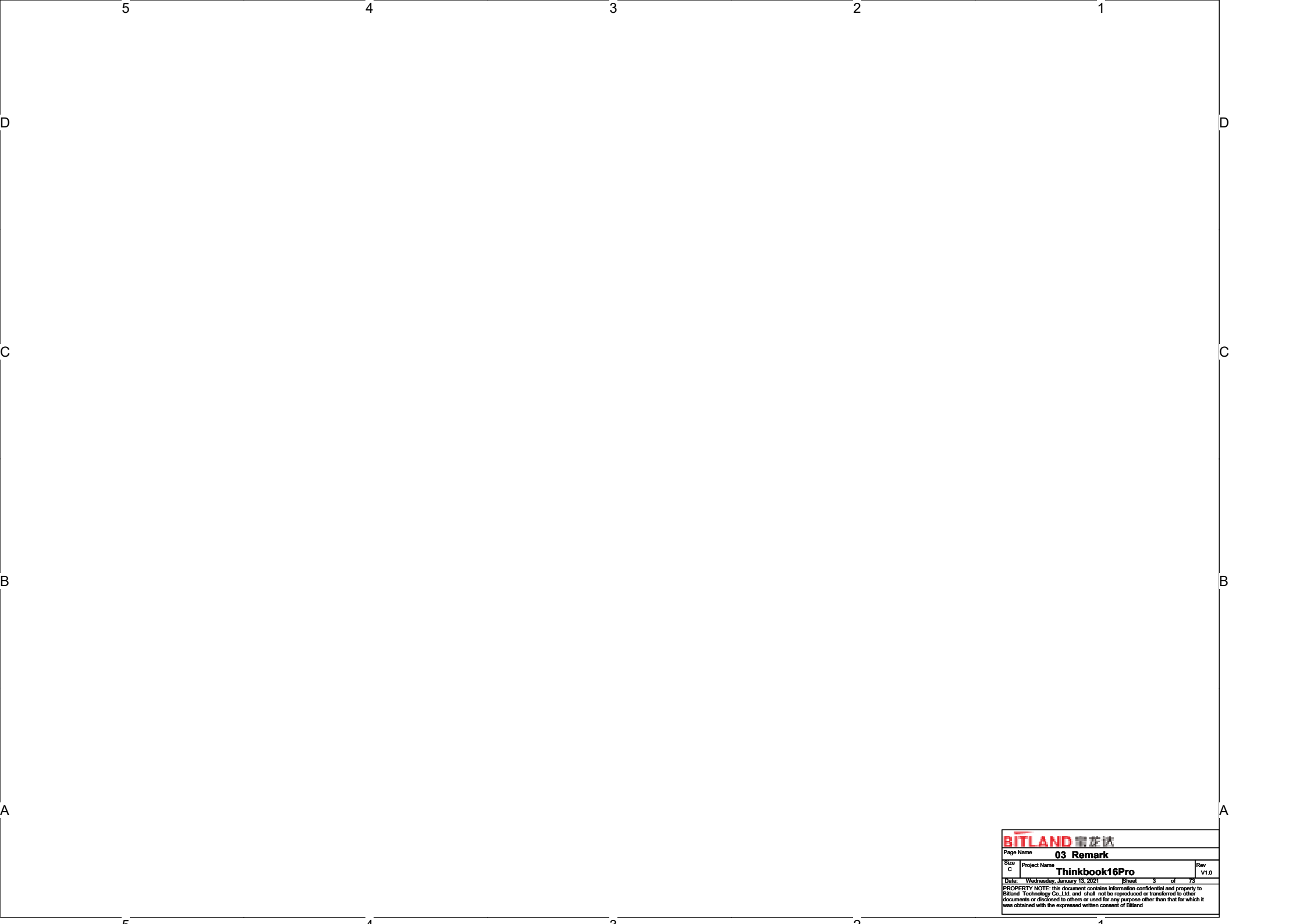
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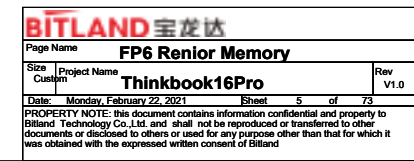
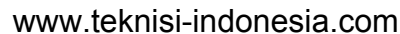
Thinkbook 16Pro System Block Diagram

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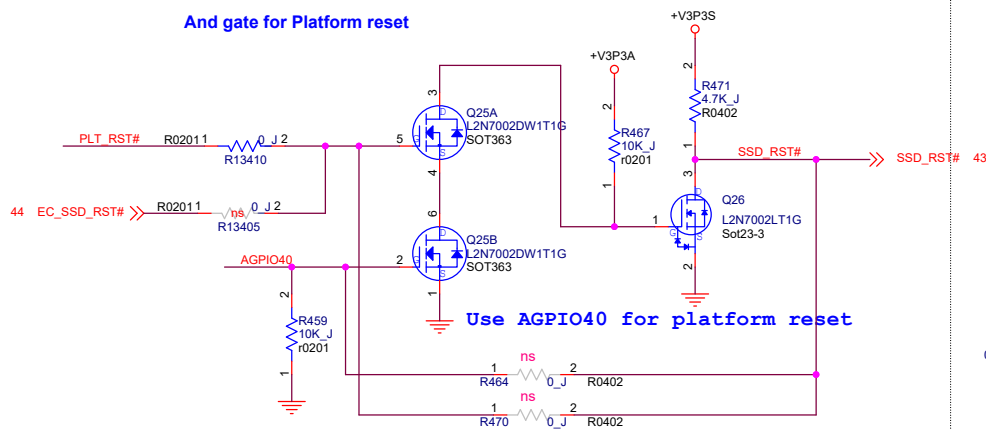




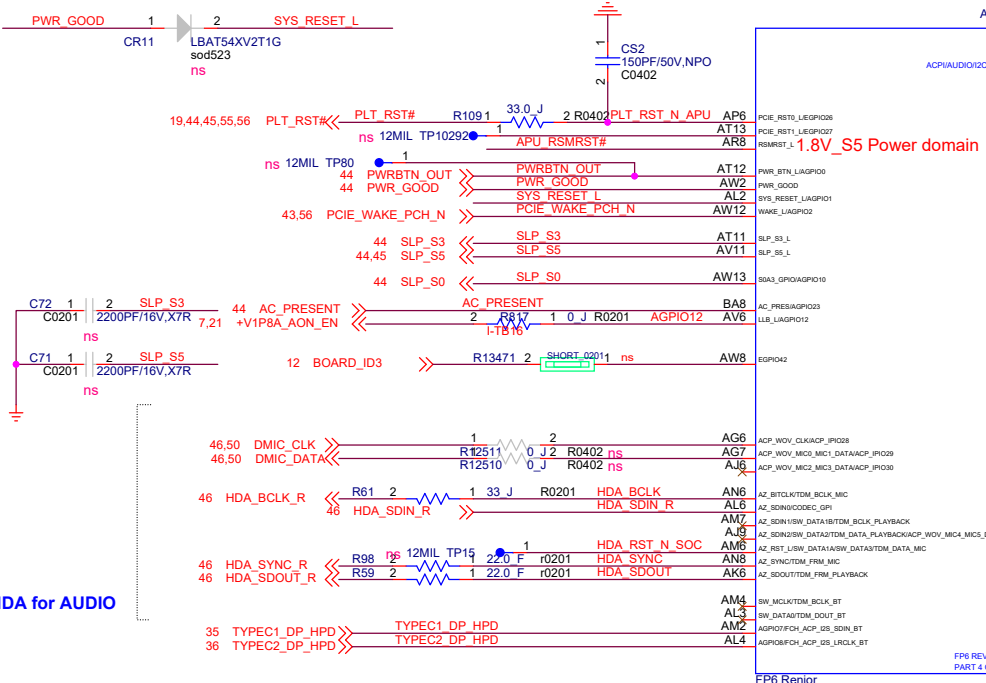
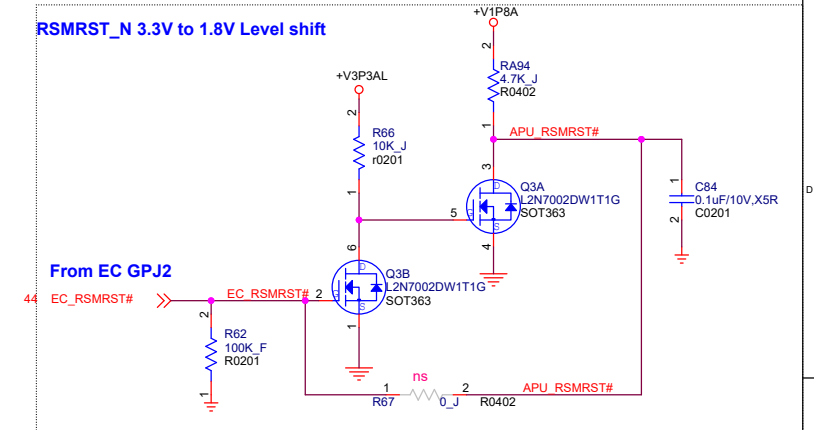
		
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And gate for Platform reset

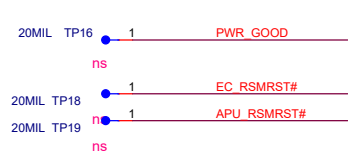


RSMRST_N 3.3V to 1.8V Level shift

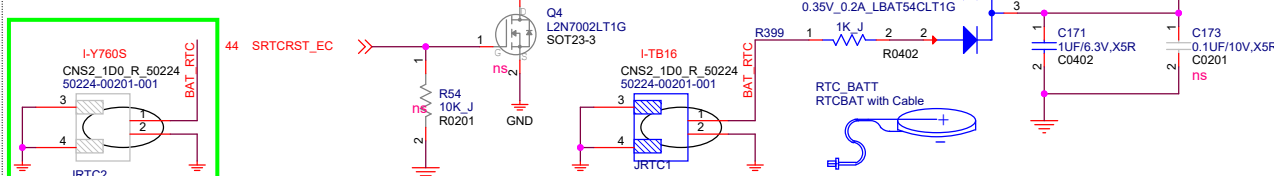


HDA for AUDIO

Test Point for debug



Clear CMOS circuit



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Page Name: **FP6 Renior SMBUS/ACPI/HDA**

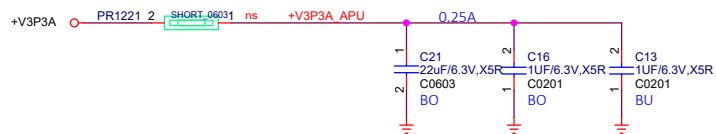
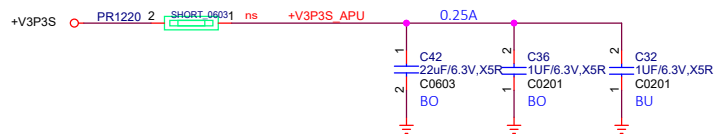
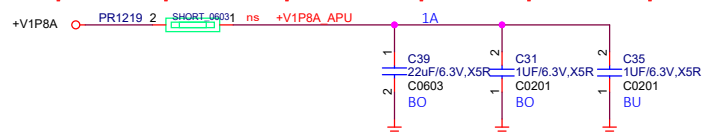
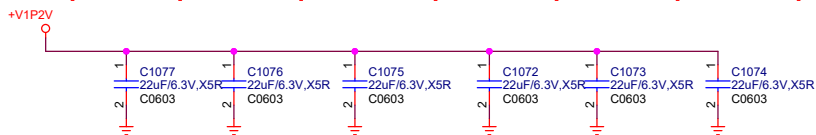
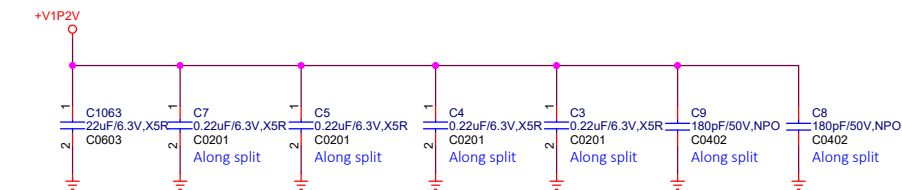
Size: **Thinkbook16Pro**

Date: **Monday, February 22, 2021**

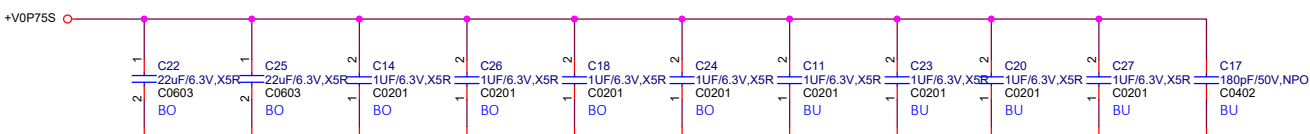
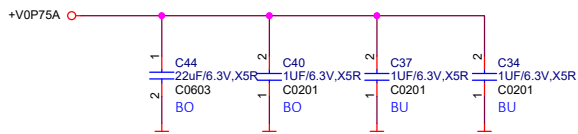
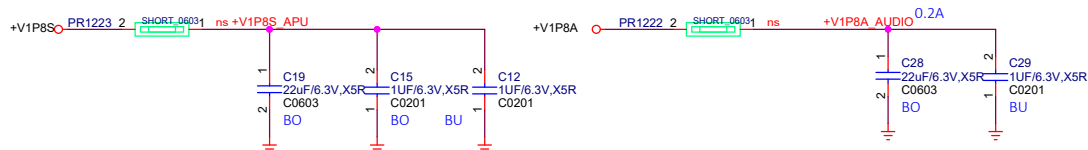
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Rev: **V1.0**

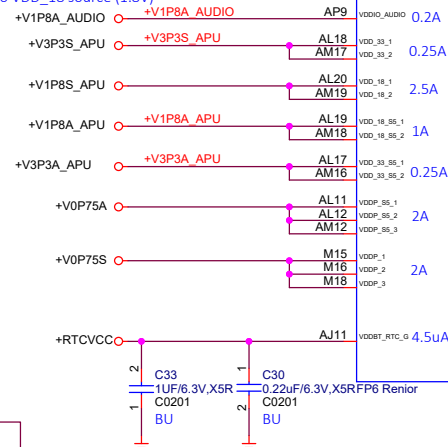
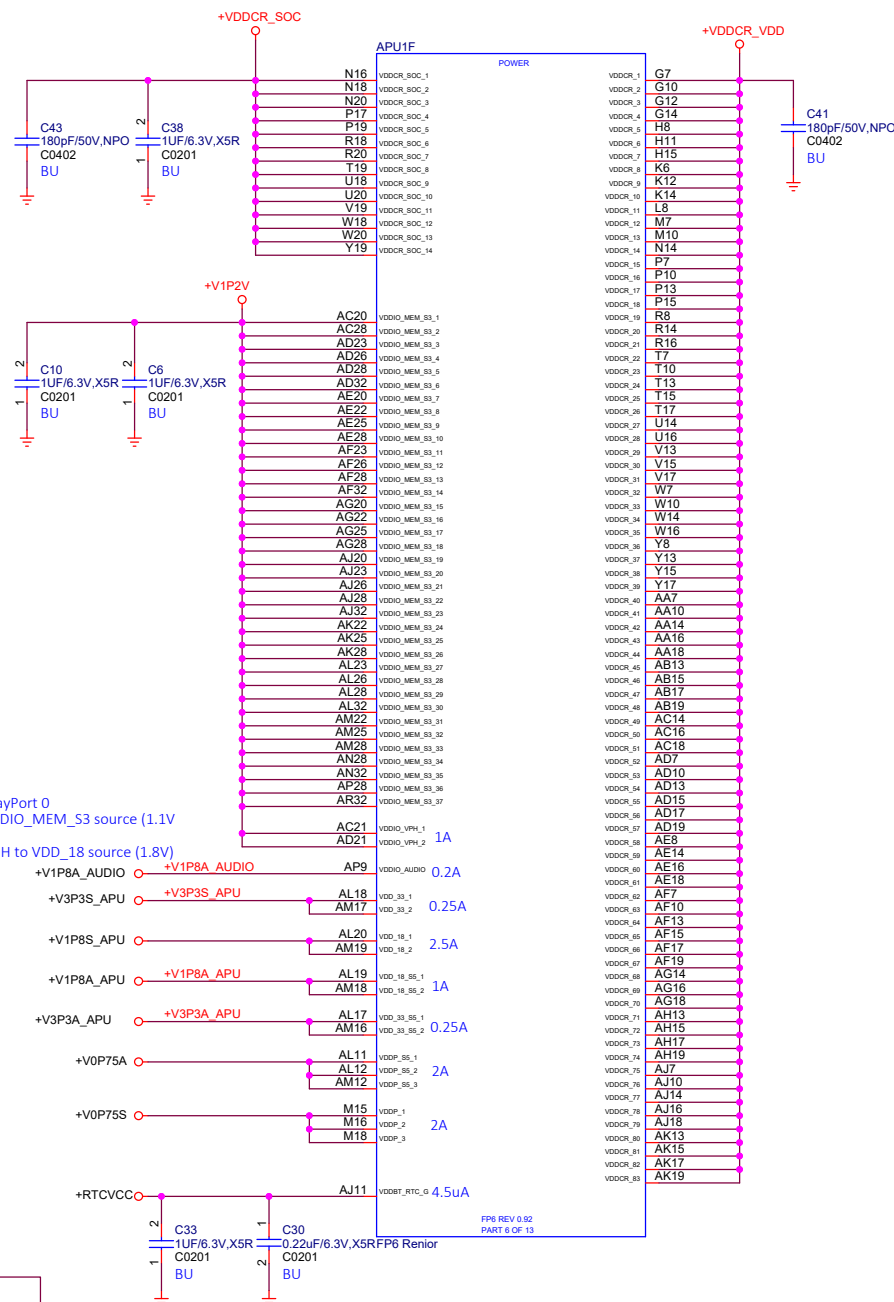
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VDDIO_VPH is a dedicated power supply for DisplayPort 0
 >>DP0 is used for eDP, connect VDDIO_VPH to VDDIO_MEM_S3 source (1.1V LPDDR4x or 1.2V DDR4) to improve battery life
 >>DP0 is used for DP or HDMI, connect VDDIO_VPH to VDD_18 source (1.8V)



BU ---> Button, under the APU
 BO ---> Button, Outside of APU



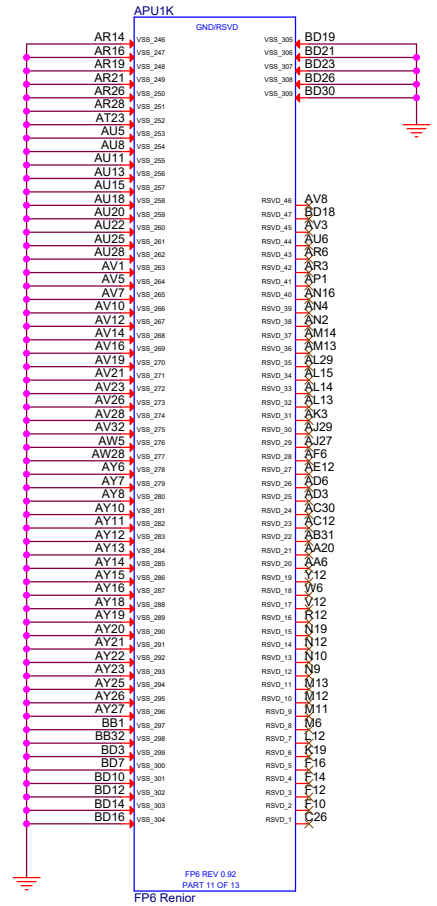
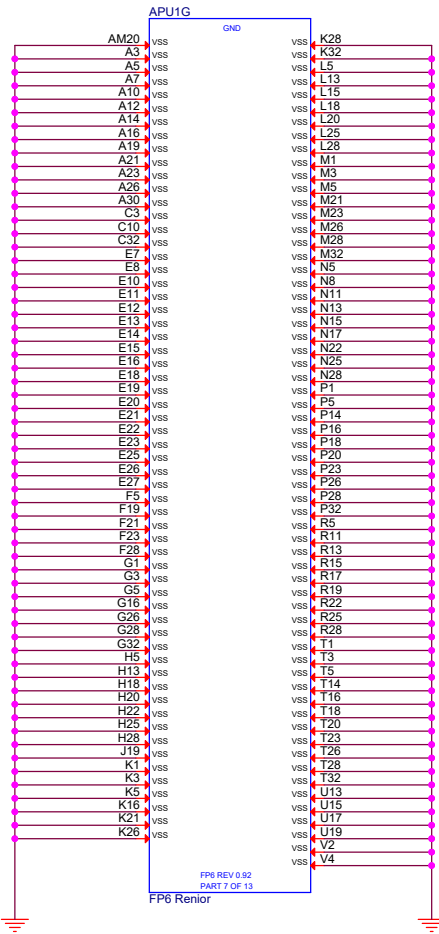
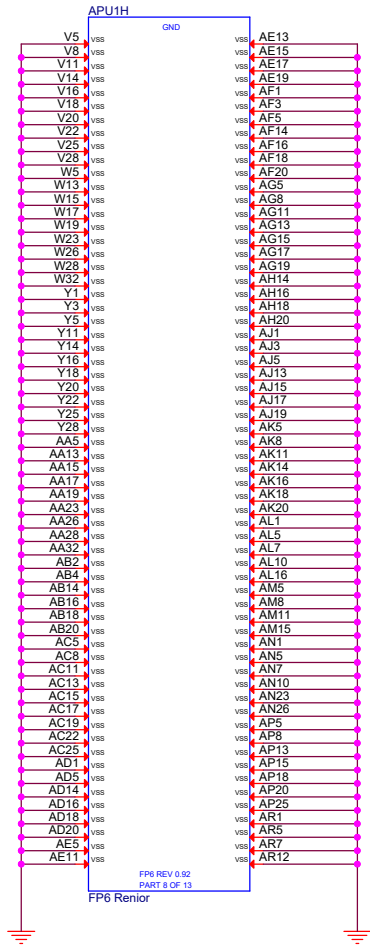
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Page Name **FP6 Renior Power**

Size Custom Project Name **Thinkbook16Pro** Rev **V1.0**

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Memory Config	EGPIO142 MEM_ID0	EGPIO140 MEM_ID1	EGPIO147 MEM_ID2	EGPIO142 BOARD_ID3	
Samsung 8Gb	0	0	0	0	0
Samsung 16Gb	1	0	0	0	1
Samsung 32Gb	0	1	0	0	2
Micron 8Gb	0	0	1	0	4
Micron 16Gb	0	0	0	1	8
Micron 32Gb	1	1	0	0	3
SK Hynix 8Gb	1	1	1	0	7
SK Hynix 16Gb	0	1	1	0	6
SK Hynix 32Gb	1	0	1	0	5
Micron 16Gb-B	1	0	0	1	9
Hynix 16Gb-JR	0	1	0	1	10

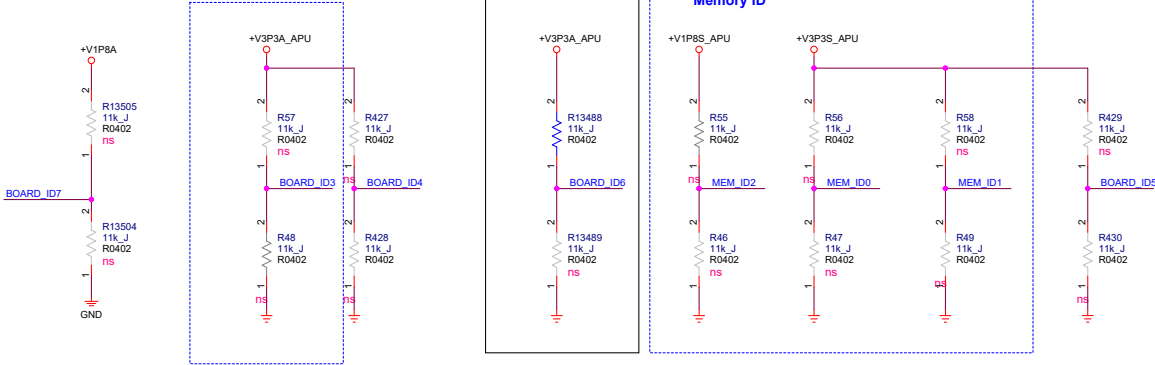
PH/PL	GPU CFG	AGPIO30 BOARD_ID7
PH	DIS	R13505
PL	UMA	R13504

PH/PL	AGPIO11 BOARD_ID4	AGPIO144 BOARD_ID5
PH	R427	R429
PL	R428	R430

GPU Config	AGPIO11 BOARD_ID4
GN20_P1	0
GN20_E3	1

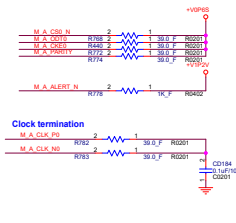
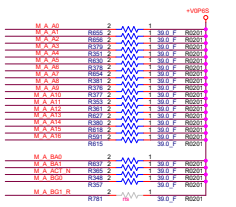
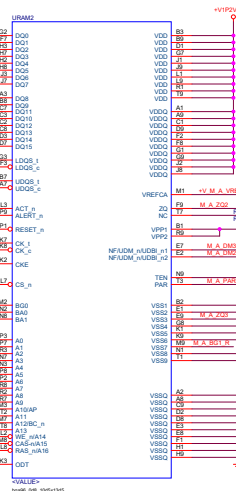
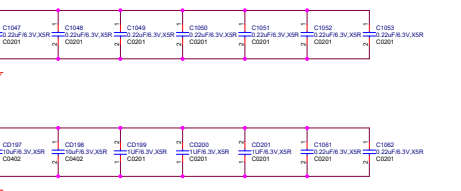
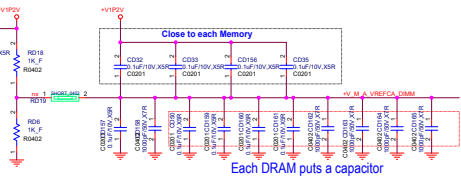
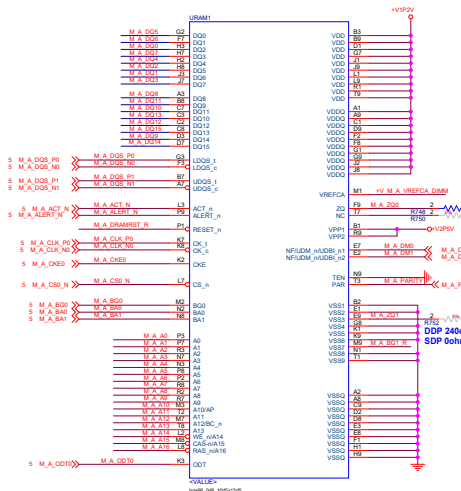
PH/PL	EGPIO142 MEM_ID0	EGPIO140 MEM_ID1	EGPIO147 MEM_ID2
PH	R56	R58	R55
PL	R47	R49	R46

MEM_ID0 >>> MEM_ID0 6
MEM_ID1 >>> MEM_ID1 6
MEM_ID2 >>> MEM_ID2 7
BOARD_ID3 >>> BOARD_ID3 7
BOARD_ID4 >>> BOARD_ID4 7
BOARD_ID5 >>> BOARD_ID5 6
BOARD_ID6 >>> BOARD_ID6 7.50
BOARD_ID7 >>> BOARD_ID7 6

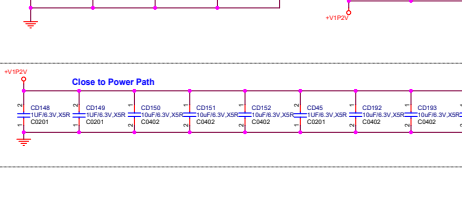
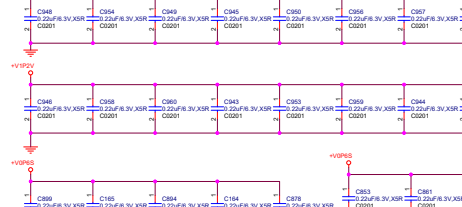
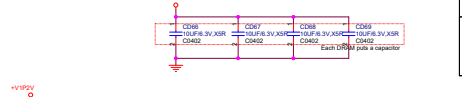
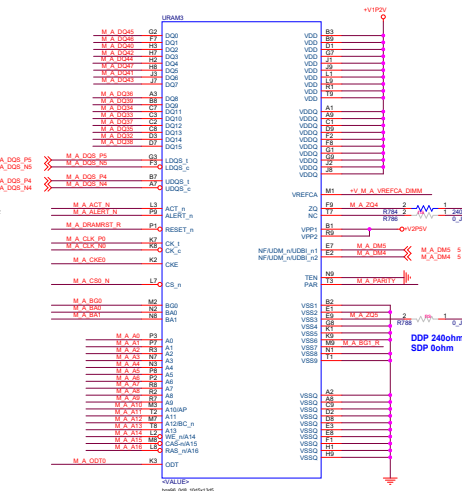


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5 M_A_DQS_P1 M_A_DQS_P1
5 M_A_AP_16 M_A_AP_16



5 M_A_DQS_P1 M_A_DQS_P1



5 M_A_DQS_P1 M_A_DQS_P1

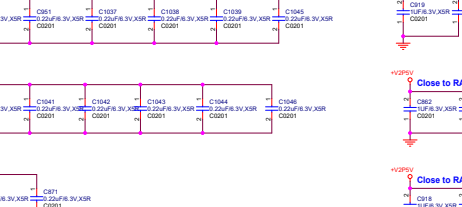
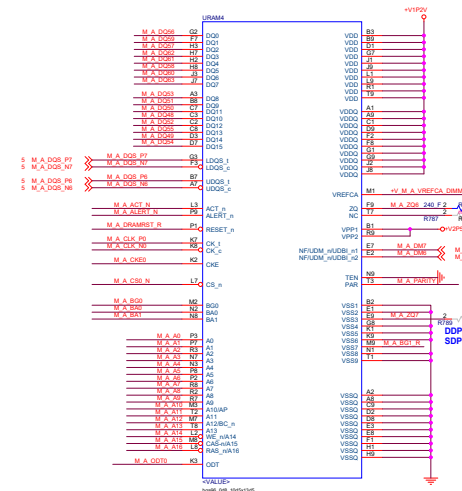
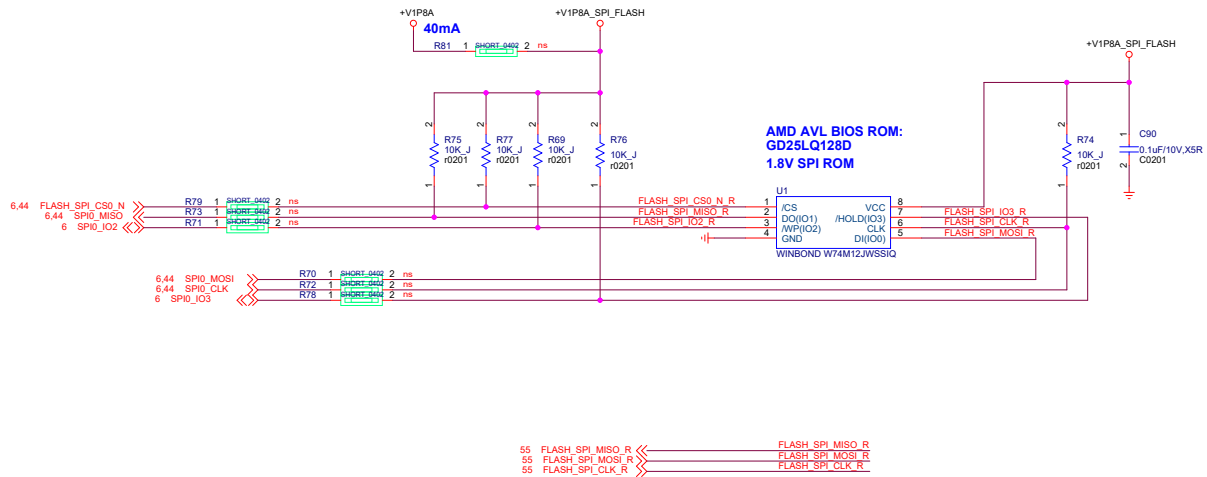


TABLE:			
	PN	SDP	DDP
R771	M9	STUFF	NS
R765		NS	STUFF
R750	T7	NC	DRAM spec
R751		NC	DRAM spec
R752		0.5%	240_1%
R753	E9	0.5%	240_1%
R754		0.5%	240_1%
R755		0.5%	240_1%



55 FLASH_SPI_MISO_R

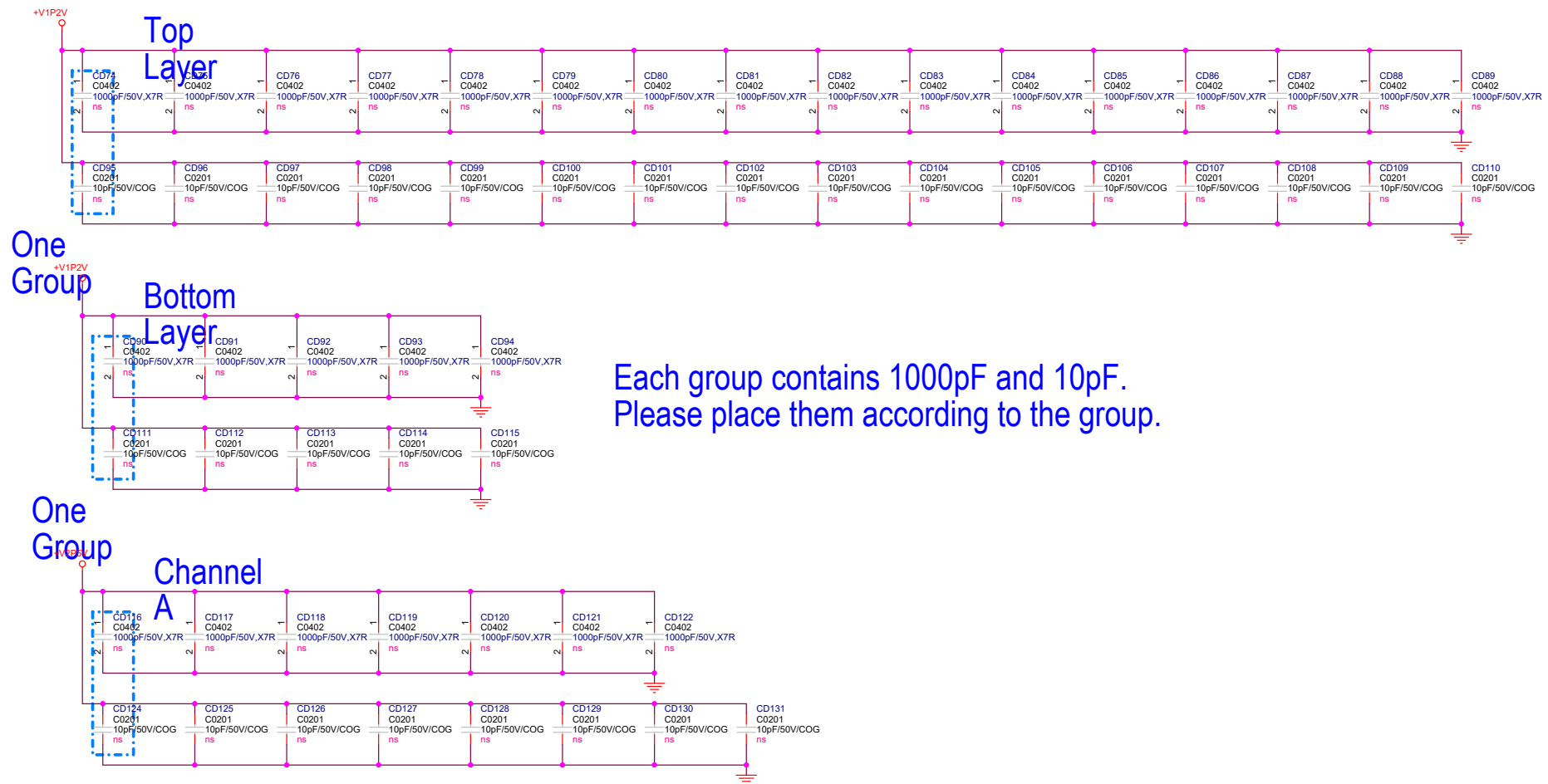
55 FLASH_SPI_MOSI_R

55 FLASH_SPI_CLK_R

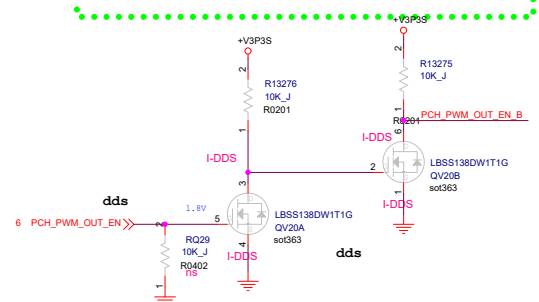
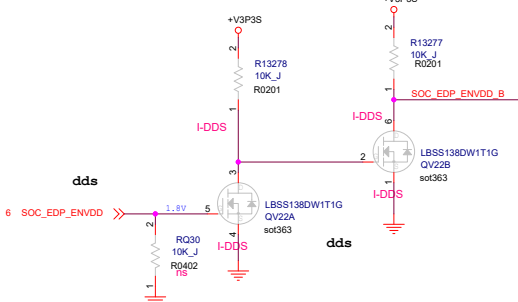
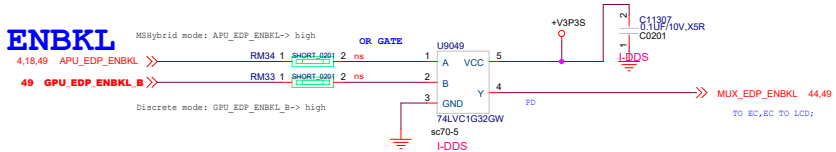
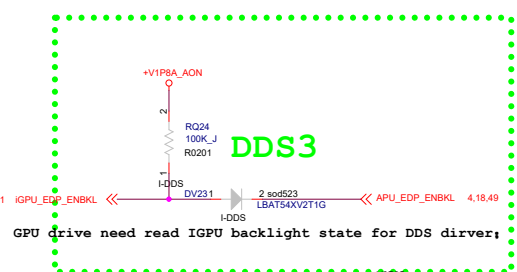
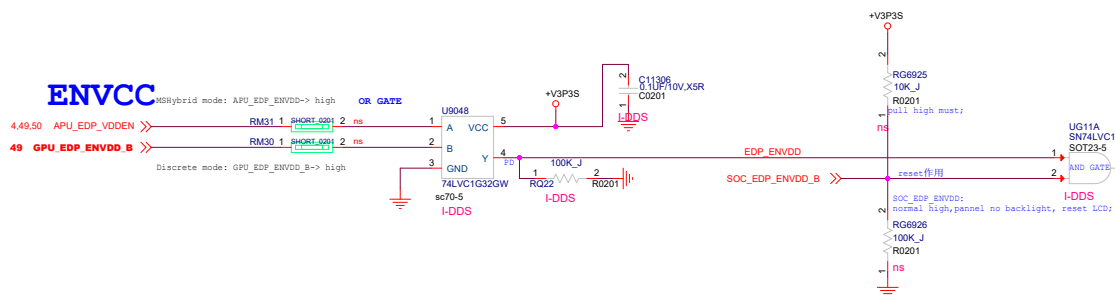
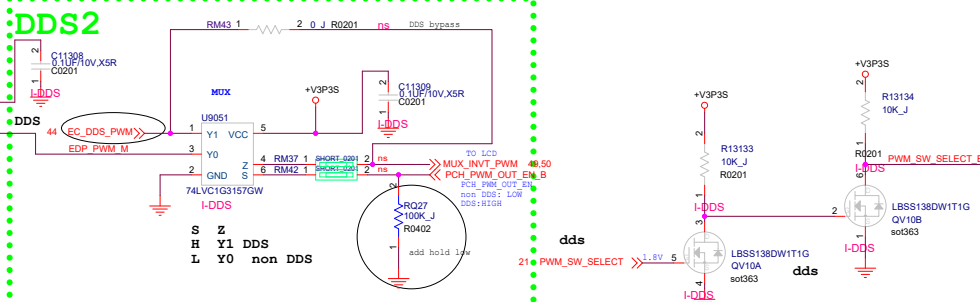
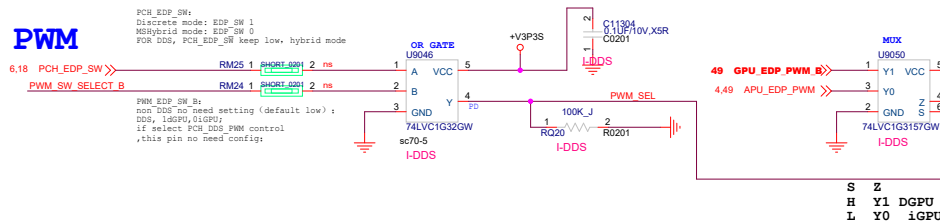
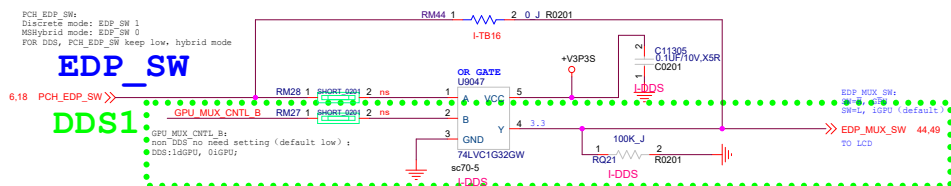
FLASH_SPI_MISO_R

FLASH_SPI_MOSI_R

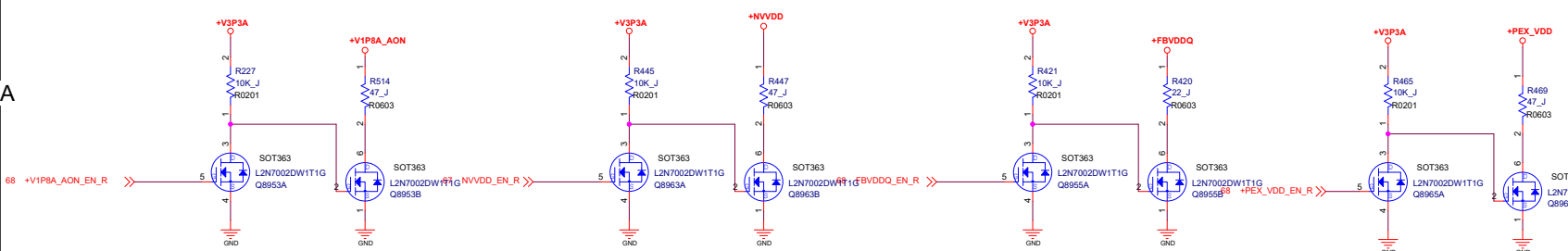
FLASH_SPI_CLK_R



DDS only support Hybrid mode
Discrete mode no support;



POWER DISCHARGE



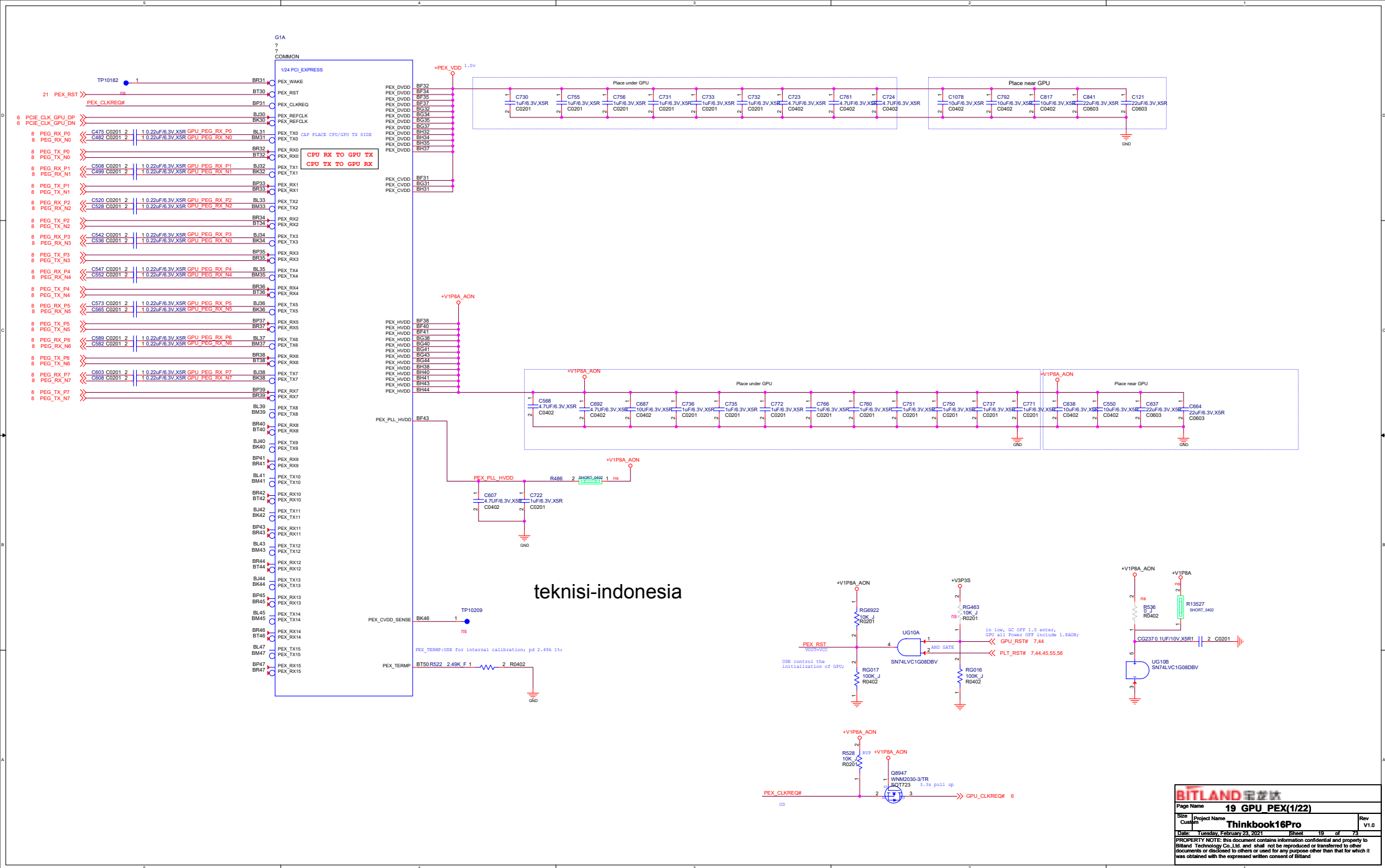


Table 9.4 GB4B-256 Standard Configurations

Link	Standard Display Configurations	
Link A	DisplayPort, DVI (Single Link)	DVI (Dual Link)
Link B	DisplayPort, DVI (Single Link)	
Link C	DisplayPort, HDMI, DVI (Single Link)	
Link D	eDP only (does not support drive of an external display)	
Link E	DisplayPort, HDMI, DVI (Single Link)	
Link F	USB-C, Dongle support for DP	

Note: Maximum of four independent simultaneously served display heads supported.
Note: eDP is supported w/o IFPD only

D

D

C

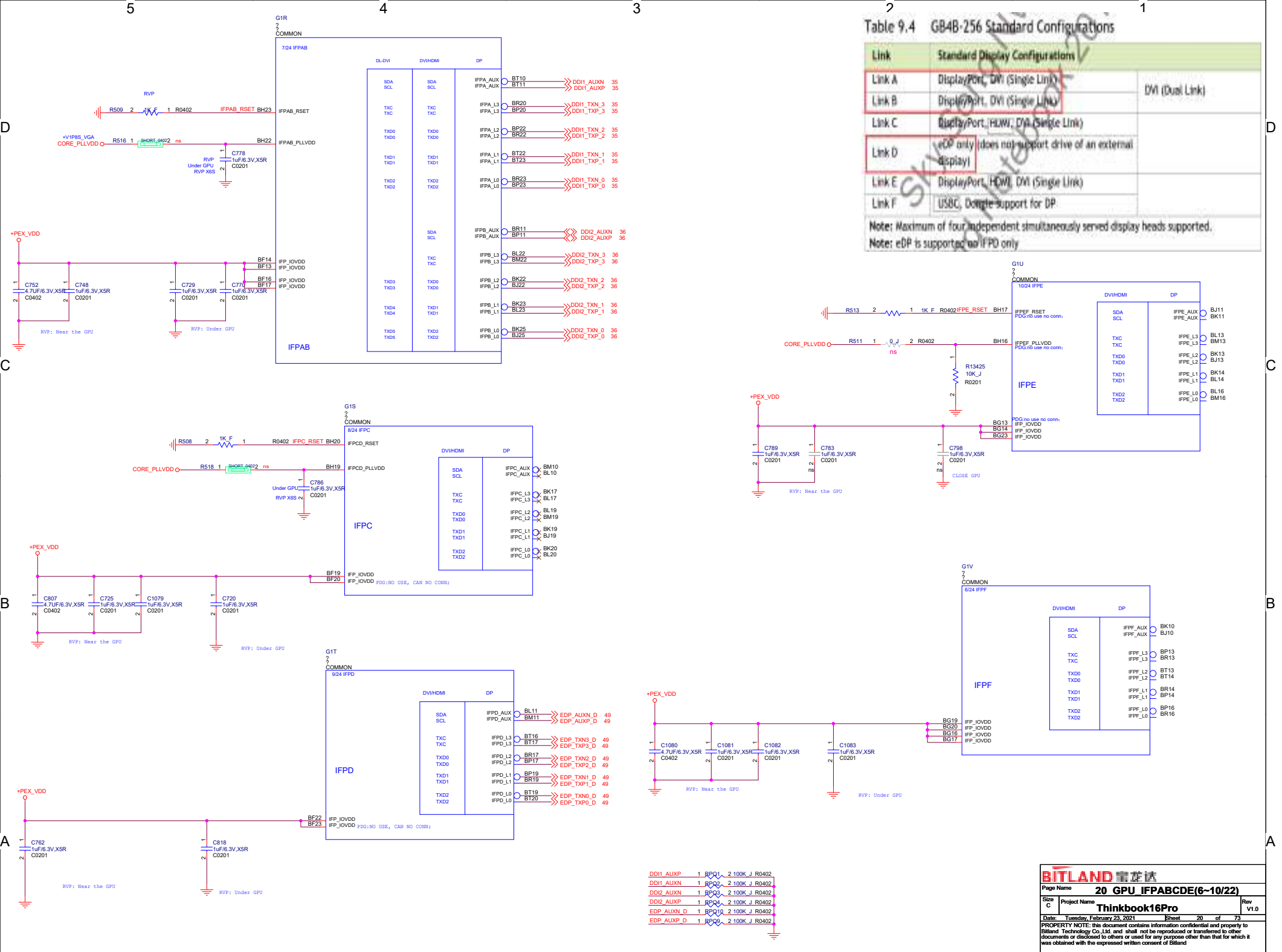
C

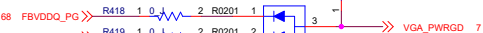
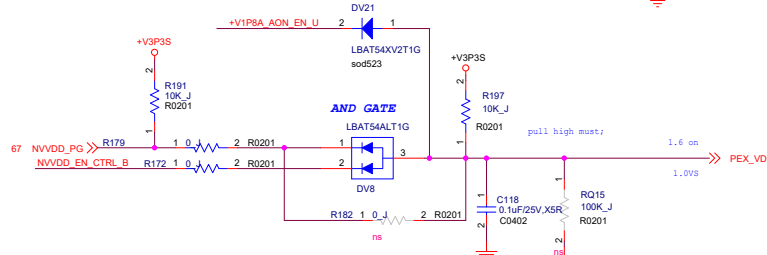
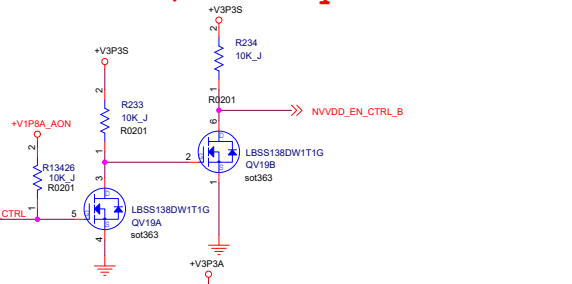
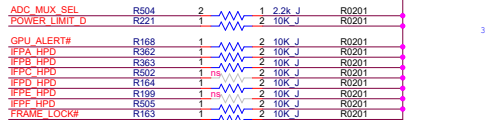
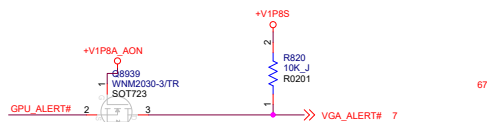
B

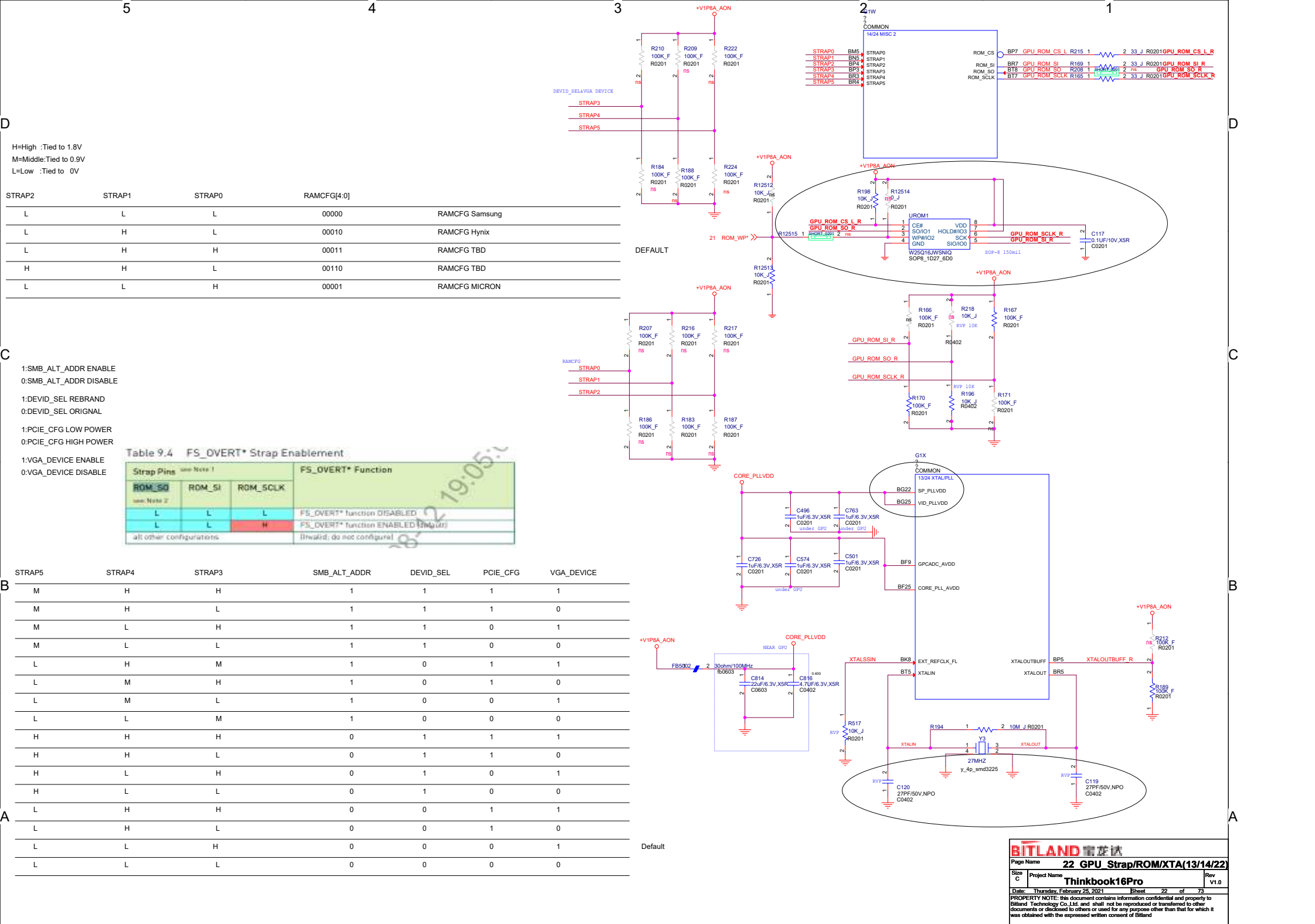
B

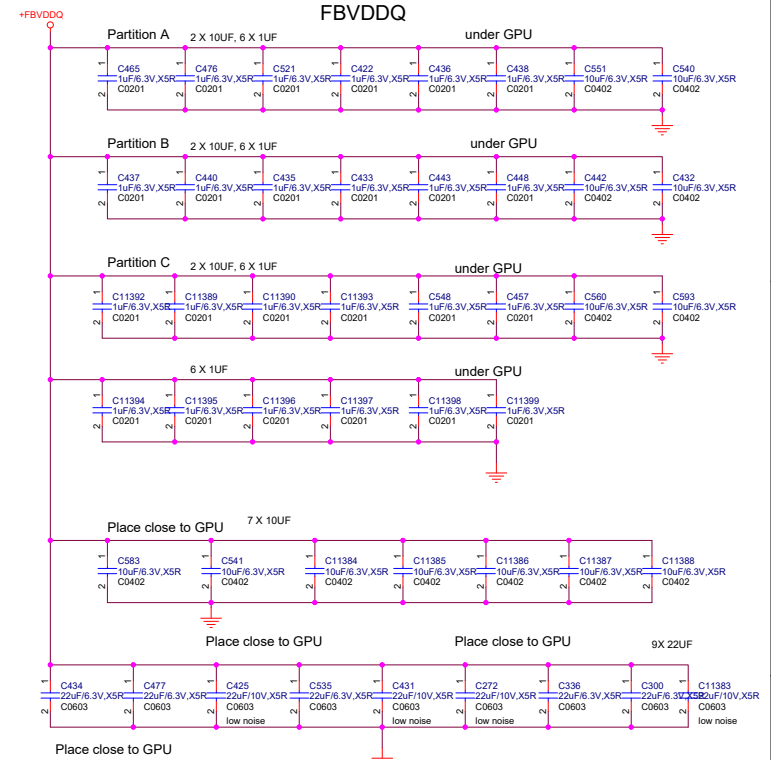
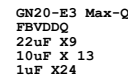
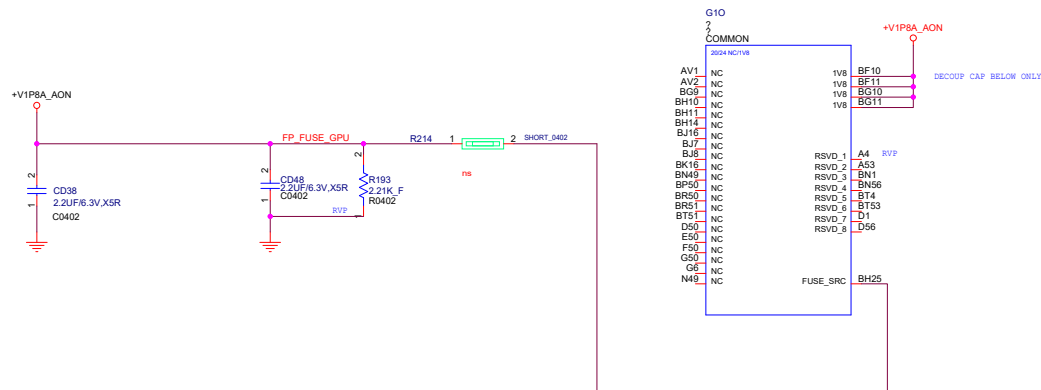
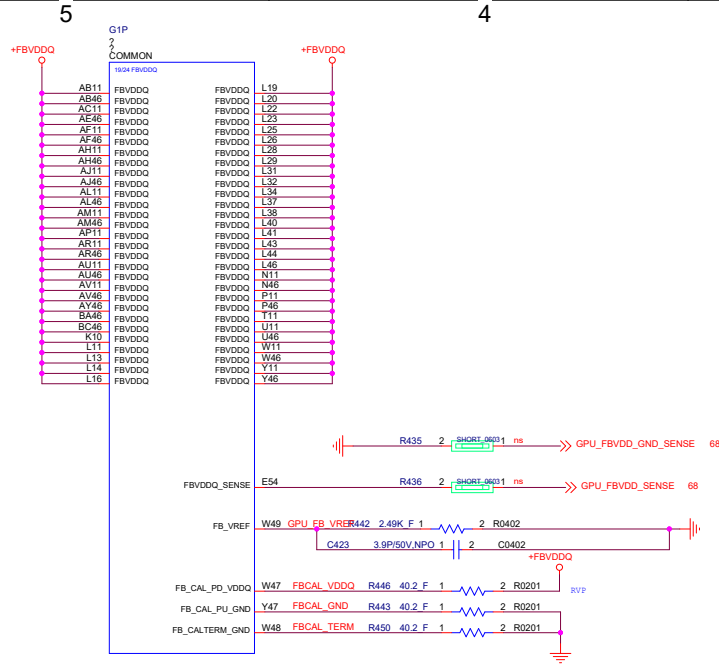
A

A

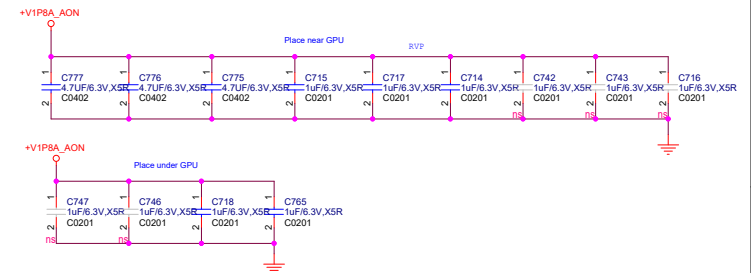


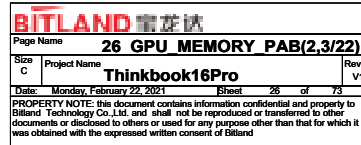


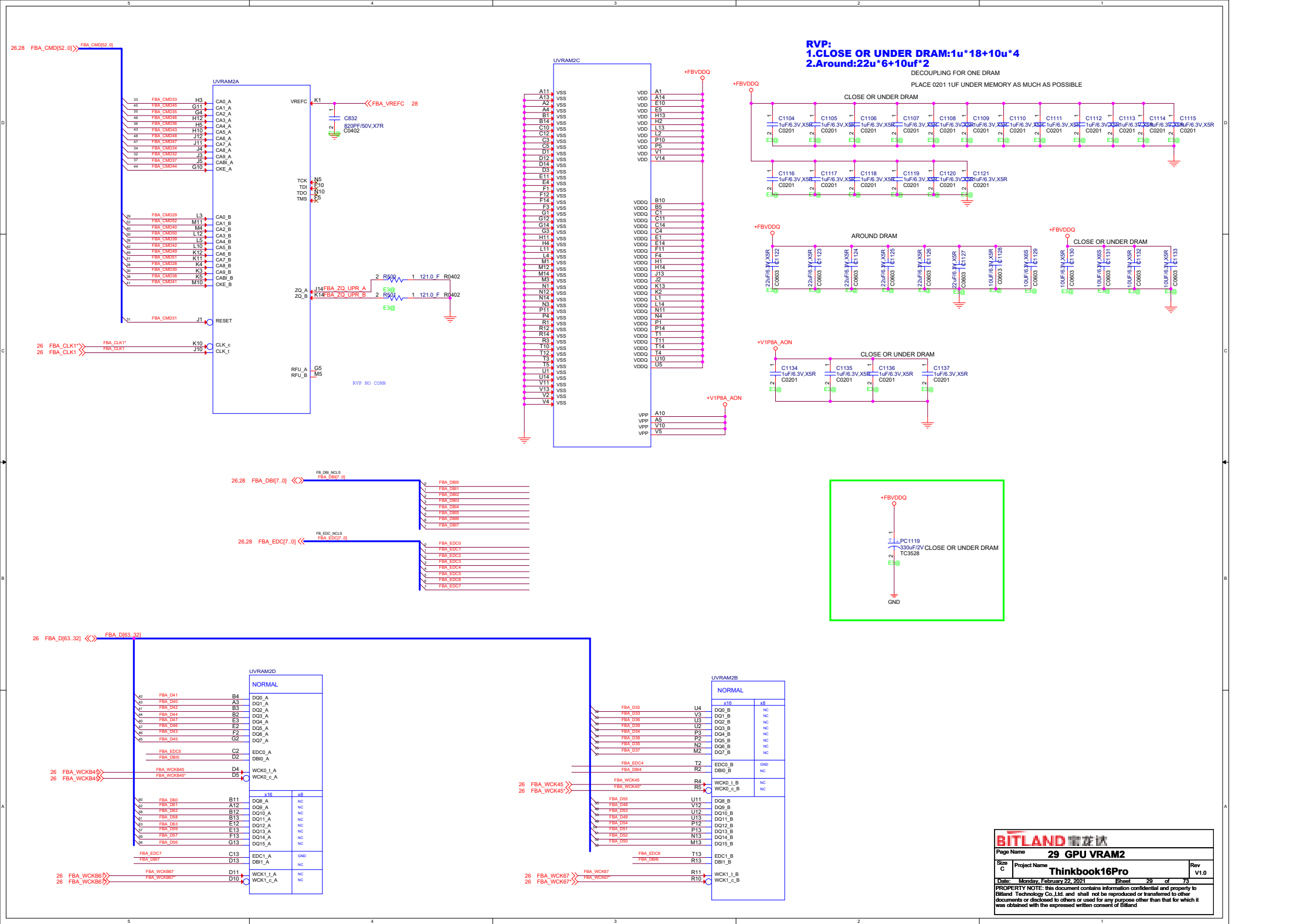


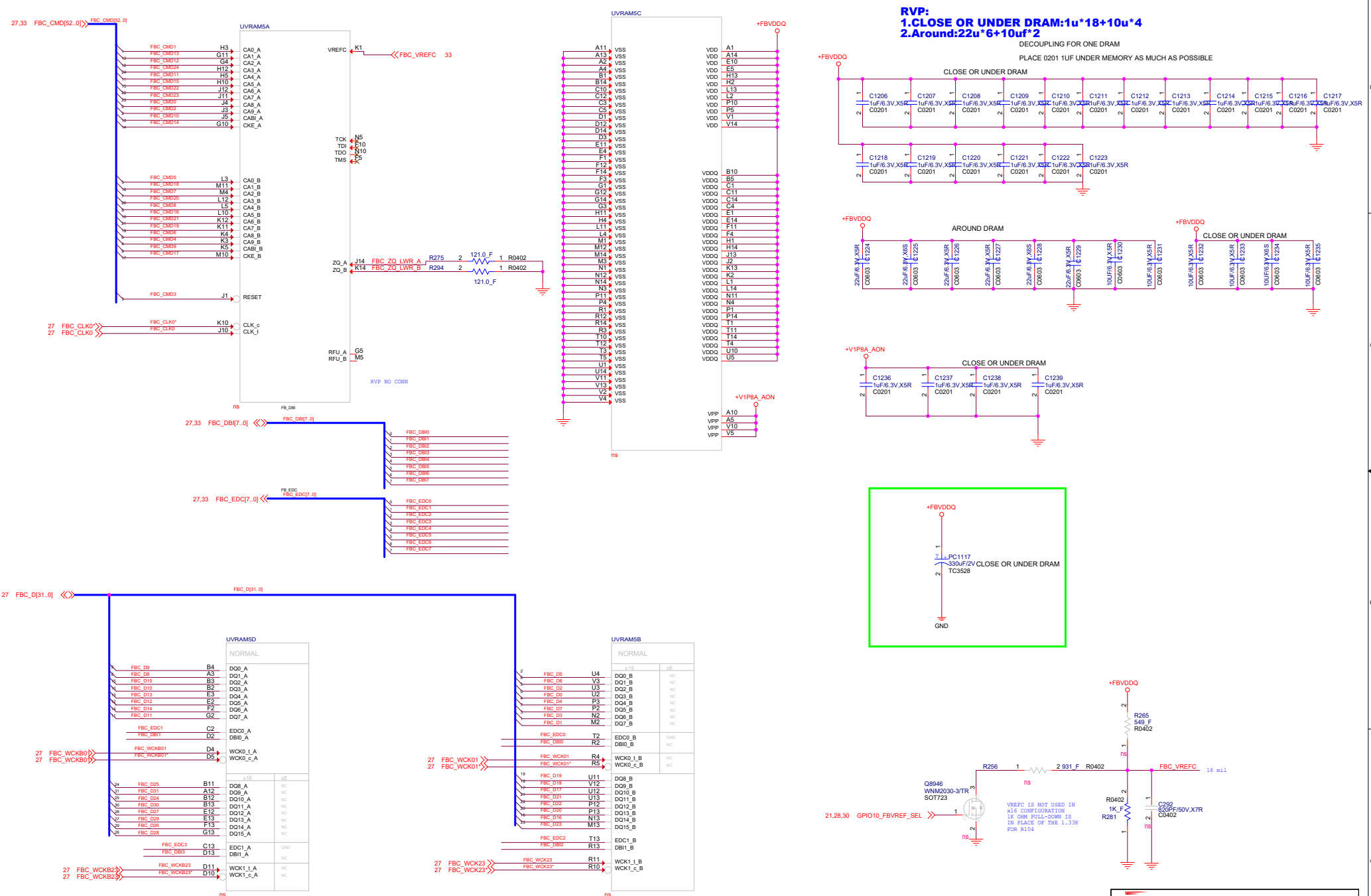


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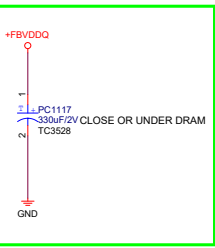
RVP:
1.CLOSE OR UNDER DRAM:1u*18+10u*4
2.Around:22u*6+10u*2

DECOUPLING FOR ONE DRAM
PLACE 0201 1uF UNDER MEMORY AS MUCH AS POSSIBLE

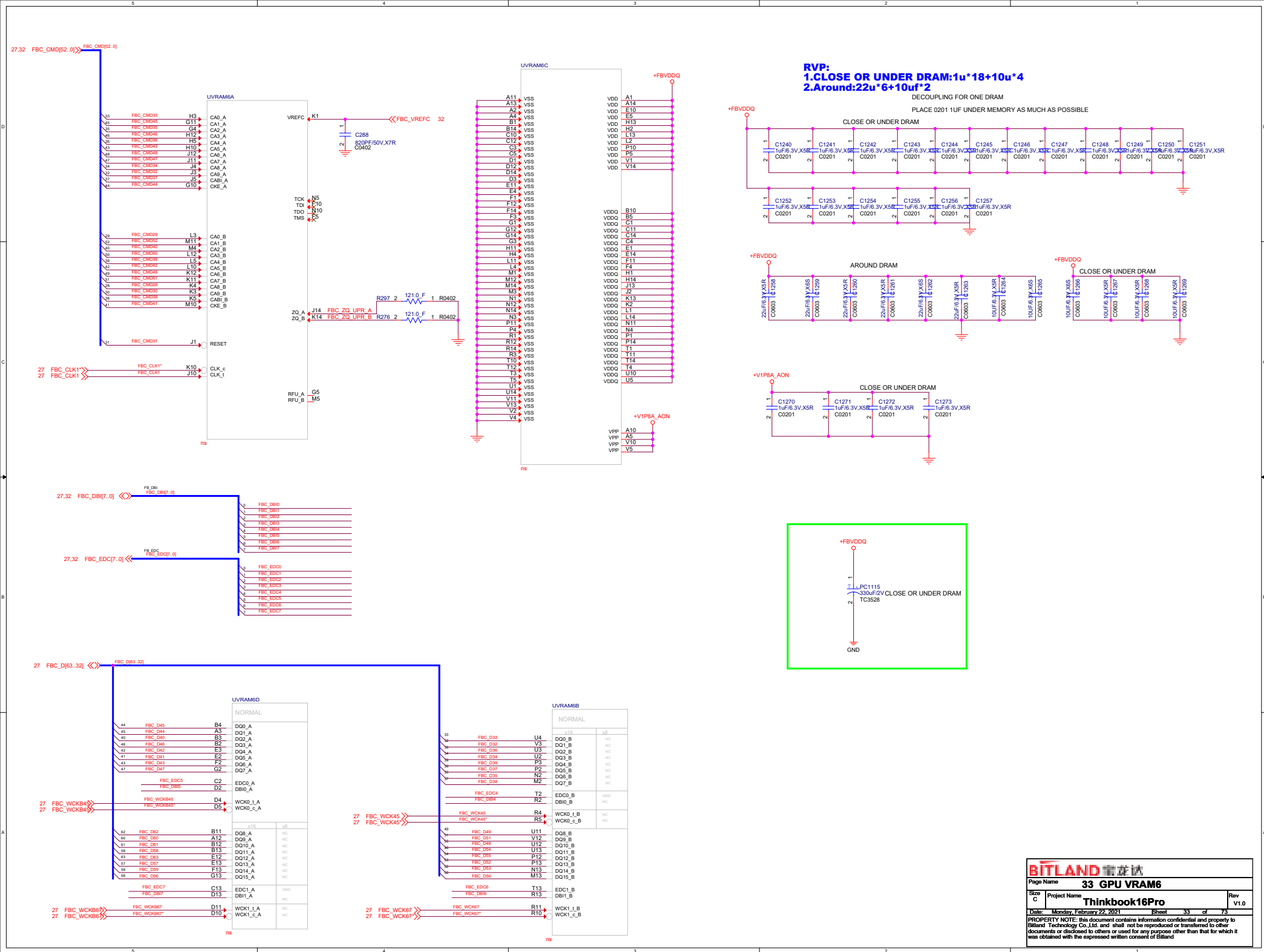
AROUND DRAM

CLOSE OR UNDER DRAM

CLOSE OR UNDER DRAM



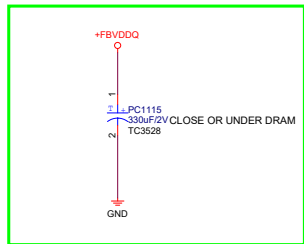
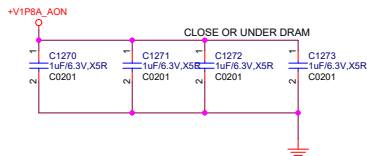
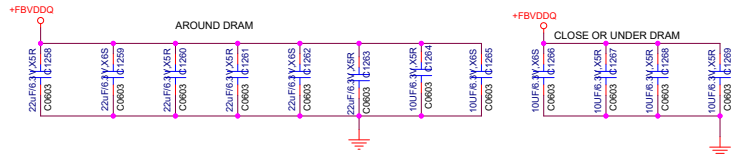
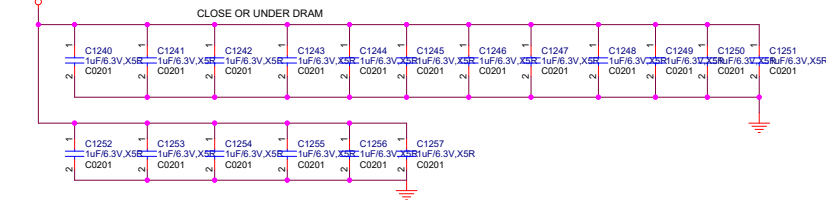
VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R104



RVP:
1.CLOSE OR UNDER DRAM:1u*18+10u*4
2.Around:22u*6+10u*2

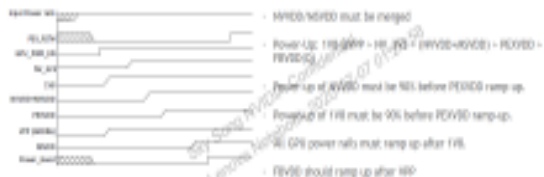
DECOUPLING FOR ONE DRAM

PLACE 0201 1UF UNDER MEMORY AS MUCH AS POSSIBLE



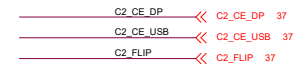
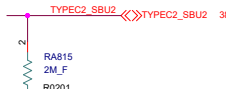
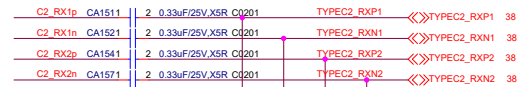
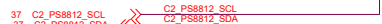
GPIO	I/O	GPIO Name	Function Description	Net name	I/O Termination
GPIO0	OUT	NVVDD_PWM_VID	PWM Output to control NVVDD	NVVDD_PWM_VID	NO PU OR PD
GPIO1	OUT	GC6:GC6_FB_EN	GC6 FRAME BUFFER ENABLE	FB_GC6_EN	(10K pull down)
GPIO2	IN	GC6:GPU_EVENT*	Wake the GPU from GC6 state	GPU_EVENT#_R	(10K pull High)
GPIO3	OUT	UNUSED	UNUSED	UNUSED	
GPIO4	OUT	GC6:1V8_MAIN_EN	GPU power sequencing for GC6 --- 1V8_MAIN_EN	1V8_MAIN_EN	(10K pull High)
GPIO5	IN	FRAME_LOCK*	Active low Frame Lock for NVSR panel	GPU_FRAME_LOCK#	(10K pull High)
GPIO6	OUT	NVVDD_PSI*	Phase Shedding, NVVDD_PSI	NVVDD_PSI	depend power topology;
GPIO7	OUT	LCD_BL_PWM	LCD Panel Backlight PWM	GPU_EDP_PWM	(100K pull down)
GPIO8	OUT	MEM_VDD_CTL	Memory voltage Control	FBVDDQ_SEL	depend DVS topology;
GPIO9	I/O	THERM_ALERT*	Active Low Thermal Alert	VGA_ALERT#	(10K pull High)
GPIO10	OUT	MEM_VREF_CTL	Memory VREF Control	MEM_VREF	(1K pull down)
GPIO11	OUT	LCD_VCC	LCD Panel VOLTAGE	GPU_EDP_ENVDD	(10K pull down)
GPIO12	IN	PWR_LEVEL	AC power detect or power supply overdraw input	VGA_AC_DET_R	(10K pull High)
GPIO13	OUT	UNUSED	UNUSED	UNUSED	
GPIO14	IN	HPD_IFPA*	Hot Plug Detect for IFPA	IFPA_HPD	(10K pull High)
GPIO15	IN	HPD_IFPB*	Hot Plug Detect for IFPB	UNUSED	(10K pull High)
GPIO16	OUT	UNUSED	UNUSED	UNUSED	
GPIO17	IN	HPD_IFPD*	Hot Plug Detect for IFPD	GPU_EDP_ENBKL	(10K pull High)
GPIO18	IN	HPD_IFPE*	Hot Plug Detect for IFPE	IFPE_HPD	(10K pull High)
GPIO19	OUT	Reserved	UNUSED	UNUSED	
GPIO20	OUT	GC6:NB_FGC6	Low Power States Fast CG6	NB_FGC6	(10K pull down)
GPIO21	OUT	LCD_BLEN	LCD Panel Backlight Enable	GPU_EDP_ENBKL	(100K pull down)
GPIO22		UNUSED	UNUSED	UNUSED	(2.2K pull High)
GPIO23		UNUSED	UNUSED	RASTER_SYNC1	(100K pull down)
GPIO24	IN	HPD_IFPF*/USBC_HPD* or DONGLE_DET*	Hot Plug Detect for IFPF or USBC	UNUSED	(10K pull High)
GPIO25	OUT	FBVDD_PSI	Turns off phases of the Frame buffer power supply	FBVDDQ_PSI	depend power topology;
GPIO26		FP_FUSE	Field-programming of select fuses	GPIO26_FP_FUSE	(10K pull down)
GPIO27	IN	HPD_IFPC*	Hot Plug Detect for IFPC	IFPC_HPD	(10K pull High)
GPIO28		ADC_MUX_SEL	OVRM MUX SEL	ADC_MUX_SEL_R	(10K pull High)
GPIO29	OUT	IDLE_IN_SW	IDLE_IN_SW	IDLE_IN_SW	(10K pull down)
GPIO30		UNUSED	UNUSED	UNUSED	

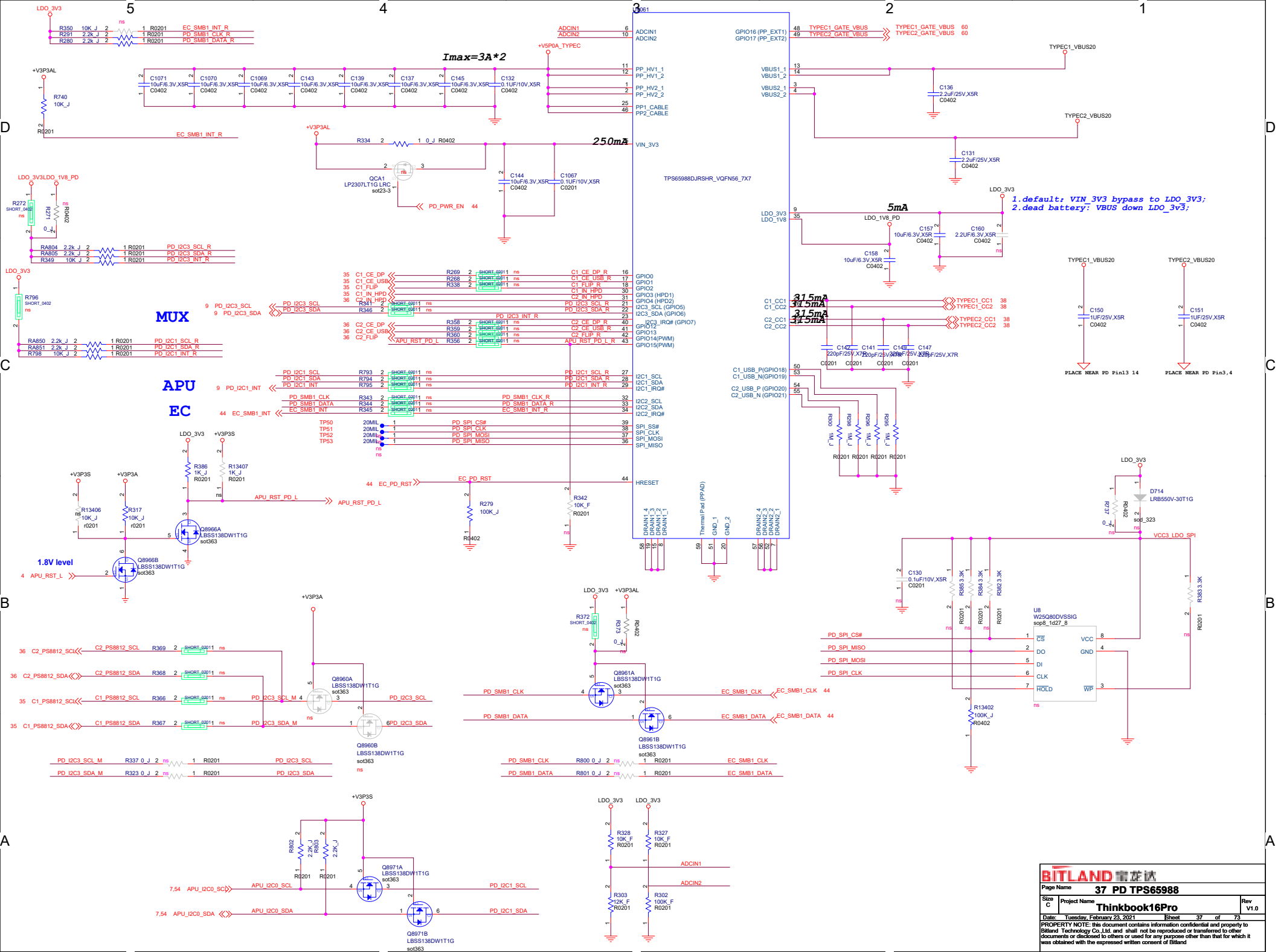
GN20X POWER DESIGN

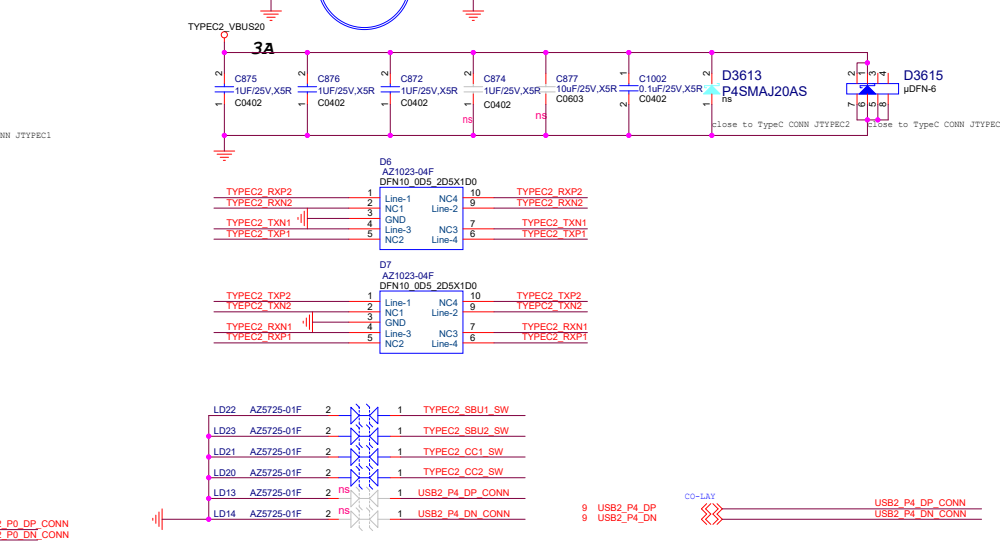
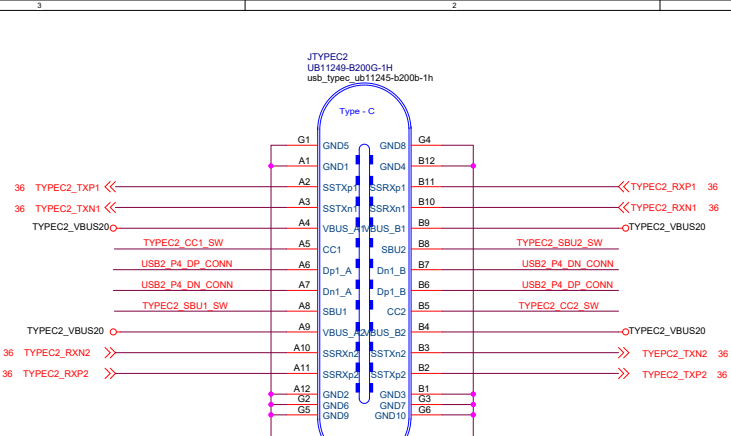
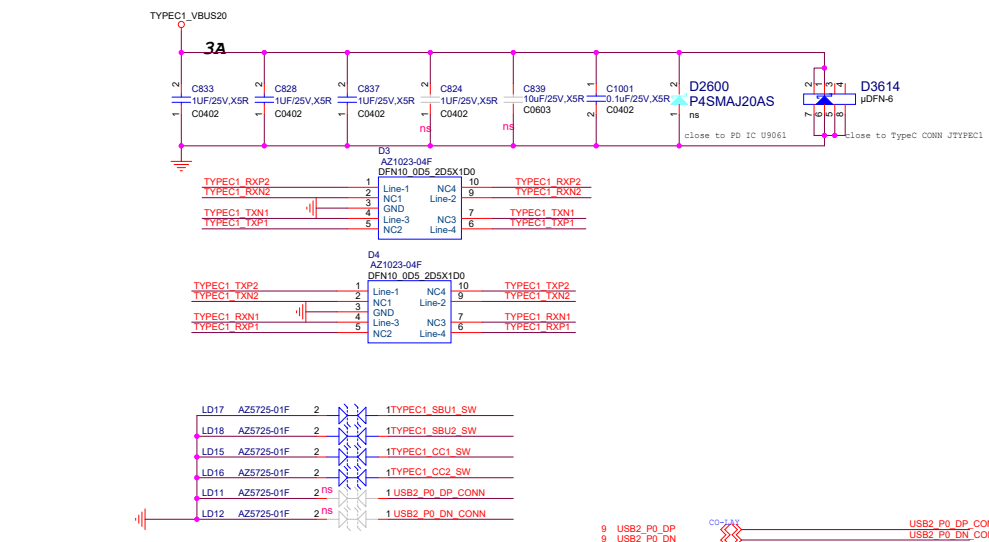
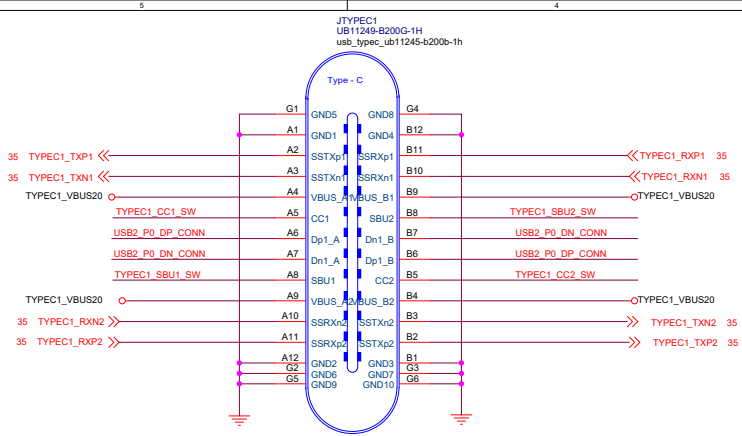
[illegible]

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]			
L	L	L	00000	RAMCFG TBD		
L	H	L	00010	RAMCFG TBD		
L	H	H	00011	RAMCFG TBD		
H	H	L	00110	RAMCFG TBD		
L	L	H	00001	RAMCFG MICRON		
H=High :Tied to 1.8V M=Middle:Tied to 0.9V L=Low :Tied to 0V						
ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0].FS_OVERT	1:ENABLE 0:DISABLE		
H	H	H	0111	FS_OVERT ENABLE		
H	H	M	0000	FS_OVERT DISABLE		
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

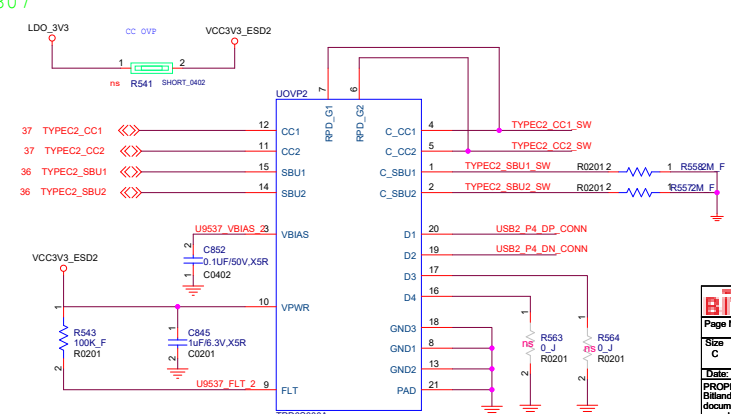
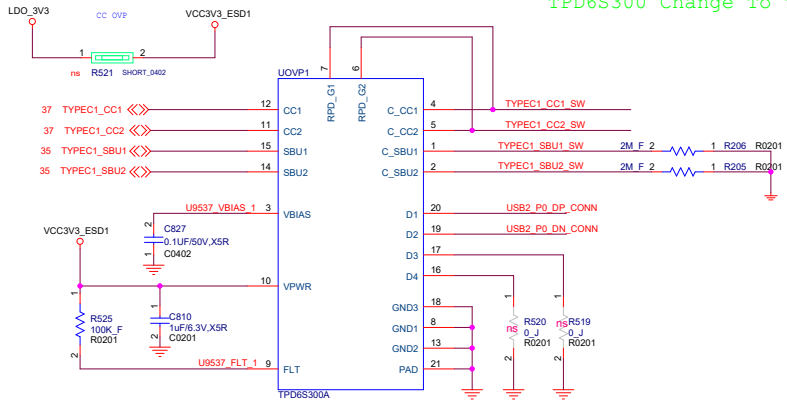
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE







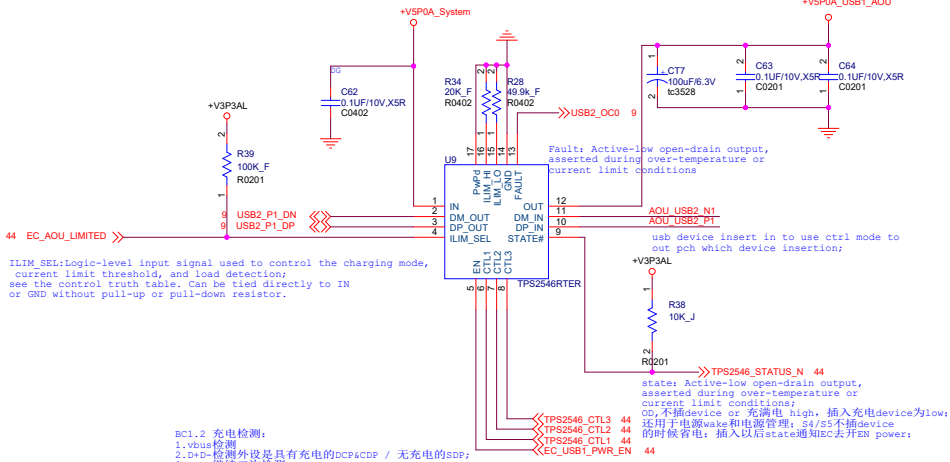
TPD6S300 Change To TPD6S300A 20200807



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Size C	Project Name Thinkbook16Pro	Rev V1.0
Date Wednesday, January 13, 2021	Sheet 39	of 73
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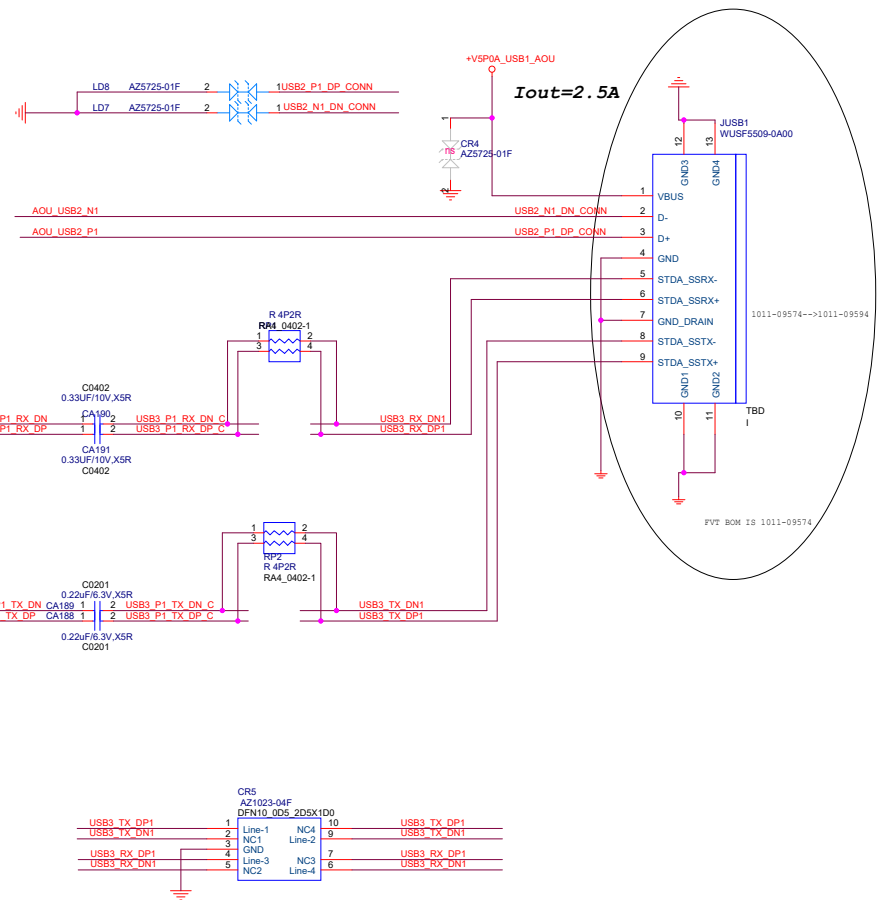
Current Limit Target:
3A (根据公式)

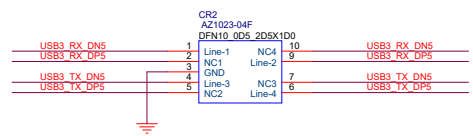
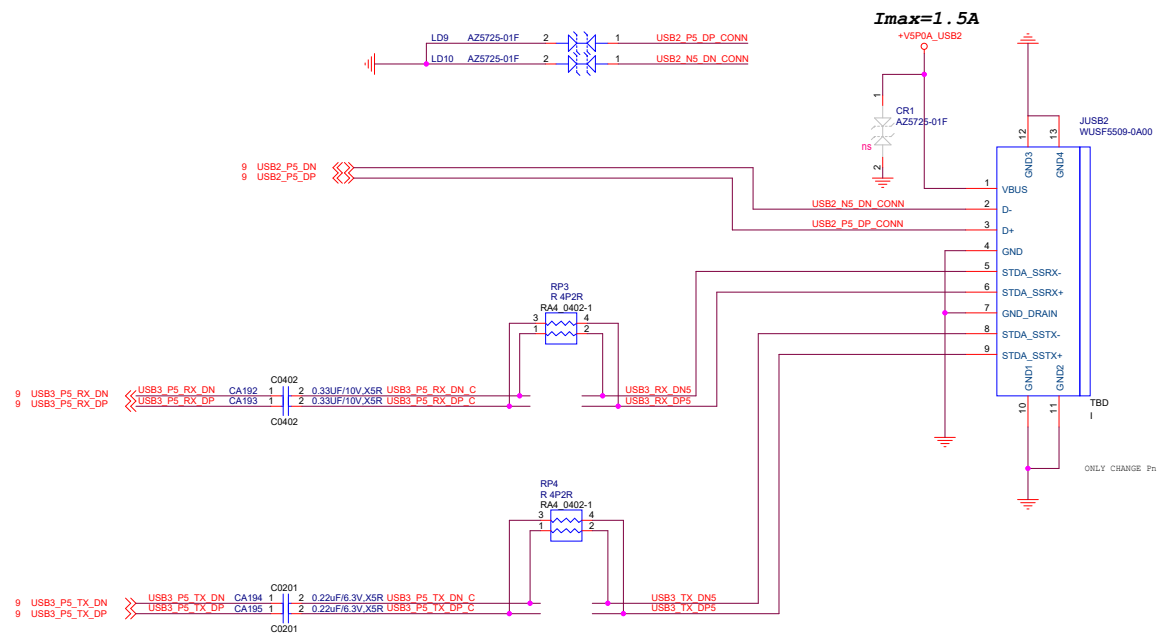
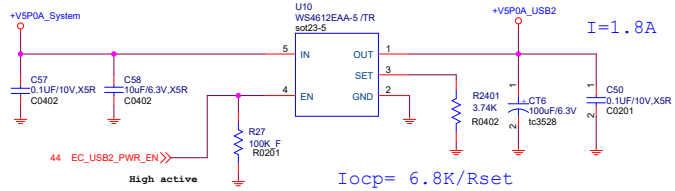


TPS2546 truth table

Input Logic Level				Mode	
CTL1	CTL2	CTL3	ILIM_SEL	Status	Current limit setting
0	0	1	1	S4/S5	DCP(Dedicated Charging Port) 专用充电端口, 无数据连接+有充电;
0	1	1	1	S3	ILIM_HI(1) 专用充电端口, 无数据连接+有充电;
1	1	1	1	S0	ILIM_HI(1) CDP(Charging Downstream Port) 充电下行端口, 有数据连接+充电;

NOTE:SDP(Standard Downstream Port) 标准下行端口, 比如鼠标, 有数据连接和电流输出+无充电
可将SDP作为传统USB端口。除USB通信外, 该端口为连接的外设提供100mA电流; 可协商达到最高500mA电流。但大多数端口通常不执行该电流限值, 不保证较高的电流。DCP不支持USB通信, 但无需任何协商即可提供超过500mA的充电电流。CDP支持USB通信和大电流充电; 该端口具有内部电路, 在充电器检测阶段打开。500mA以上端口(CDP和CDP)与500mA以下端口(SDP)
(1) IOS_PW: Current limit (IOS) is automatically switched between IOS_PW (S4/S5, no device or full charge 55mA) and the value set by ILIM_HI according to the Load Detect Power Wake Functionality.





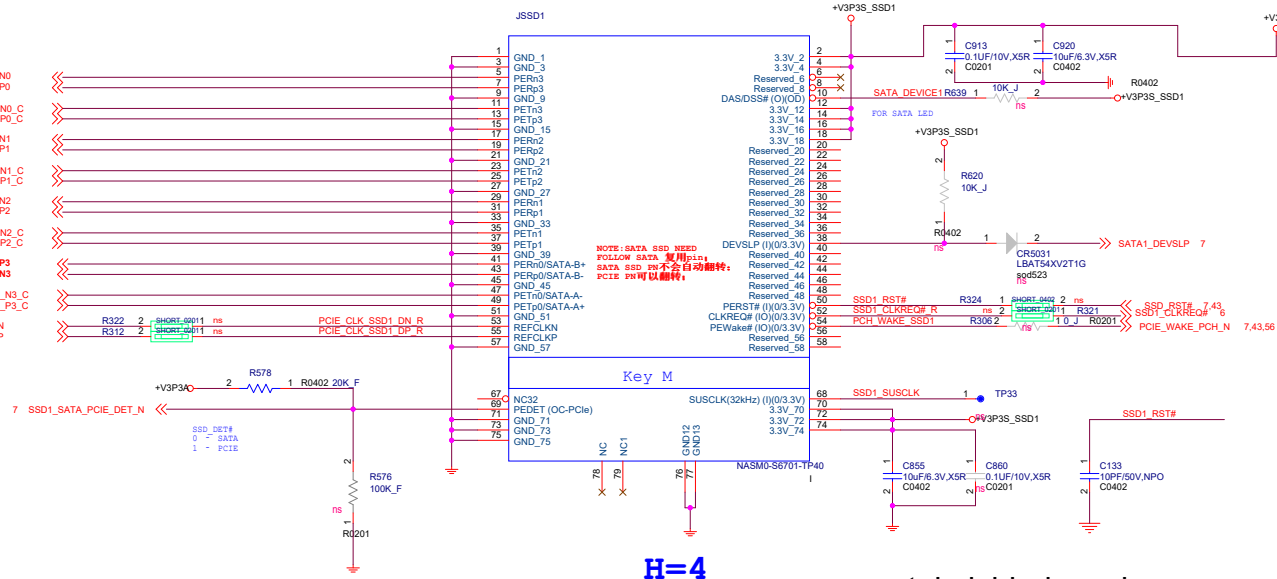


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Date: <u>Wednesday, January 13, 2021</u> Sheet: <u>42</u> of <u>73</u>		
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D

D

8 PCIE_SSD_RX_N0
8 PCIE_SSD_RX_P0
8 PCIE_SSD_TX_N0_C
8 PCIE_SSD_TX_P0_C
8 PCIE_SSD_RX_N1
8 PCIE_SSD_RX_P1
8 PCIE_SSD_TX_N1_C
8 PCIE_SSD_TX_P1_C
8 PCIE_SSD_RX_N2
8 PCIE_SSD_RX_P2
8 PCIE_SSD_TX_N2_C
8 PCIE_SSD_TX_P2_C
8 PCIE_SSD_RX_P3
8 PCIE_SSD_RX_N3
8 PCIE_SSD_TX_N3_C
8 PCIE_SSD_TX_P3_C
6 PCIE_CLK_SSD1_DN
6 PCIE_CLK_SSD1_DP



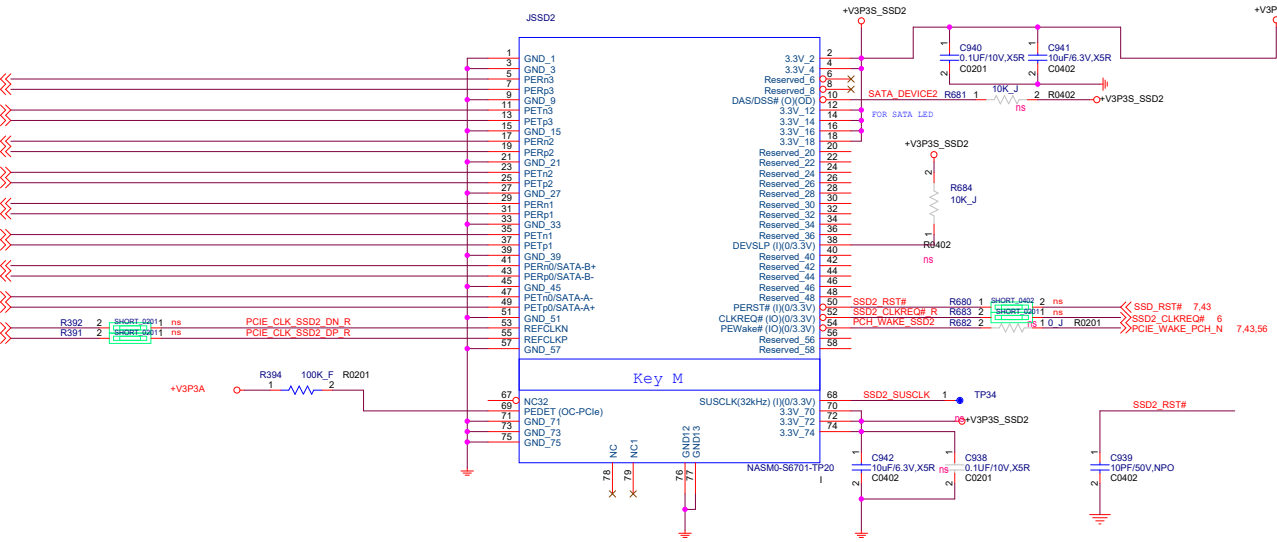
H=4

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B

B

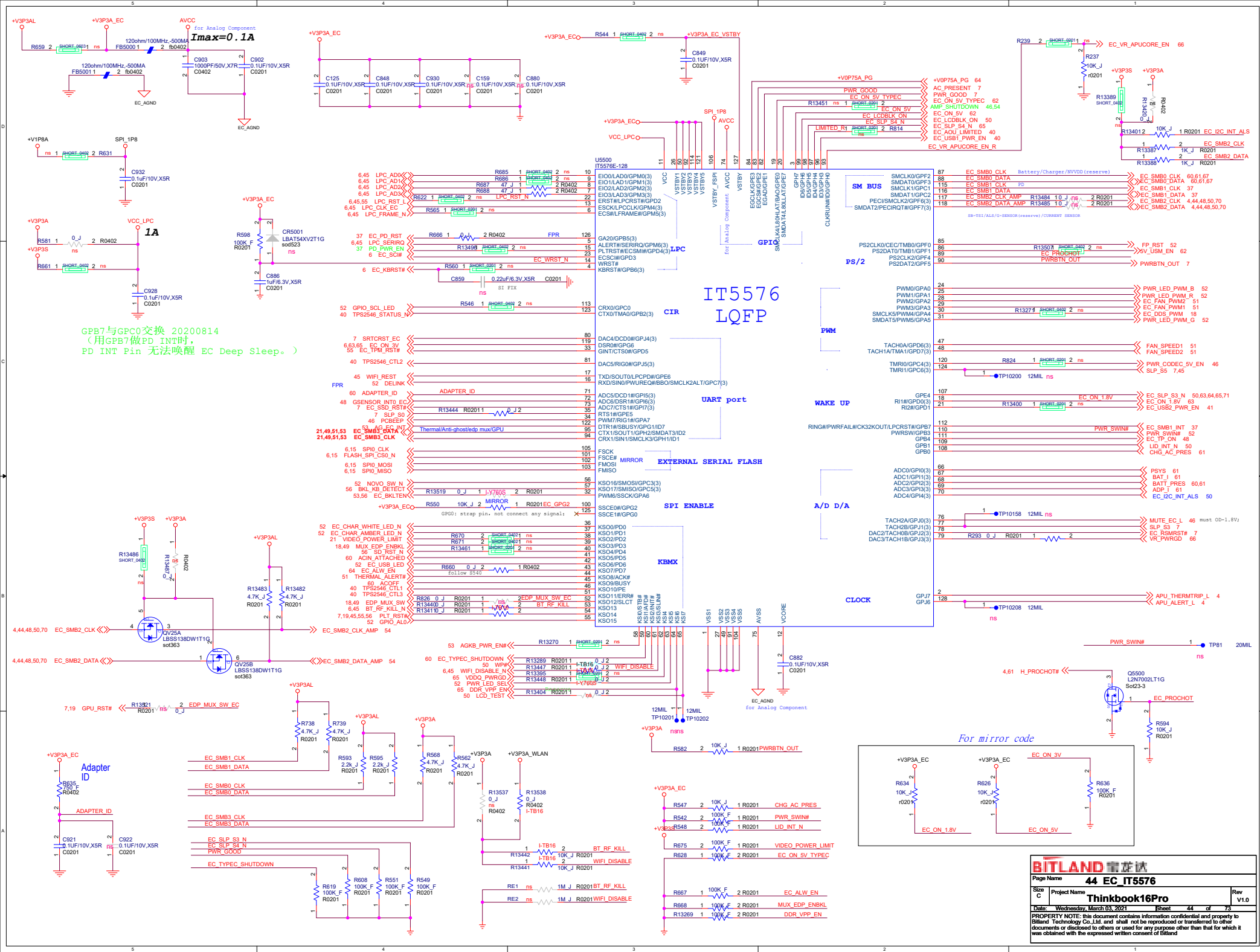
8 PCIE_SSD_RX_N11
8 PCIE_SSD_RX_P11
8 PCIE_SSD_TX_N11_C
8 PCIE_SSD_TX_P11_C
8 PCIE_SSD_RX_N10
8 PCIE_SSD_RX_P10
8 PCIE_SSD_TX_N10_C
8 PCIE_SSD_TX_P10_C
8 PCIE_SSD_RX_N9
8 PCIE_SSD_RX_P9
8 PCIE_SSD_TX_N9_C
8 PCIE_SSD_TX_P9_C
8 PCIE_SSD_RX_N8
8 PCIE_SSD_RX_P8
8 PCIE_SSD_TX_N8_C
8 PCIE_SSD_TX_P8_C
6 PCIE_CLK_SSD2_DN
6 PCIE_CLK_SSD2_DP

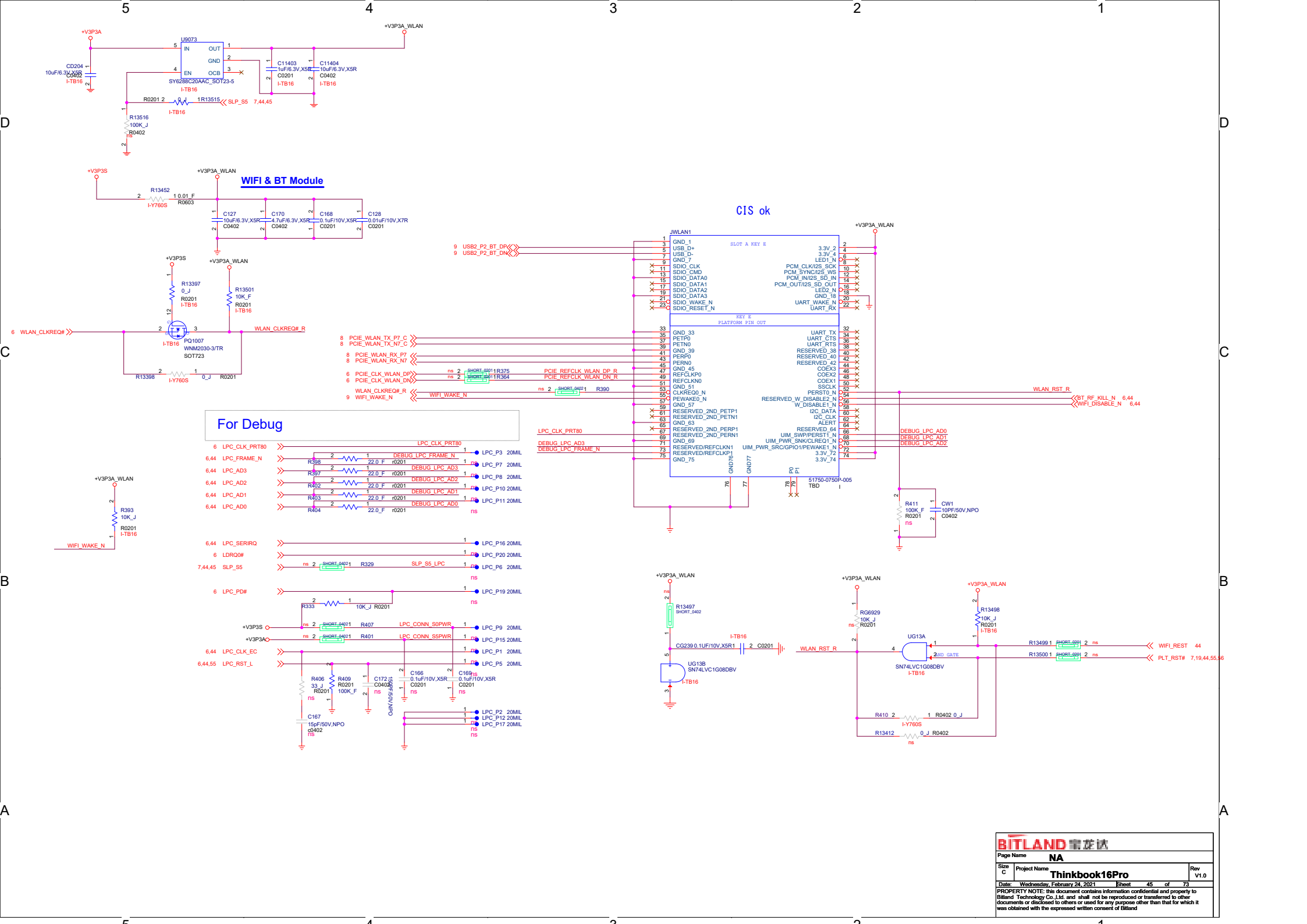


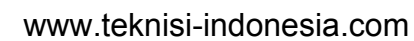
H=2

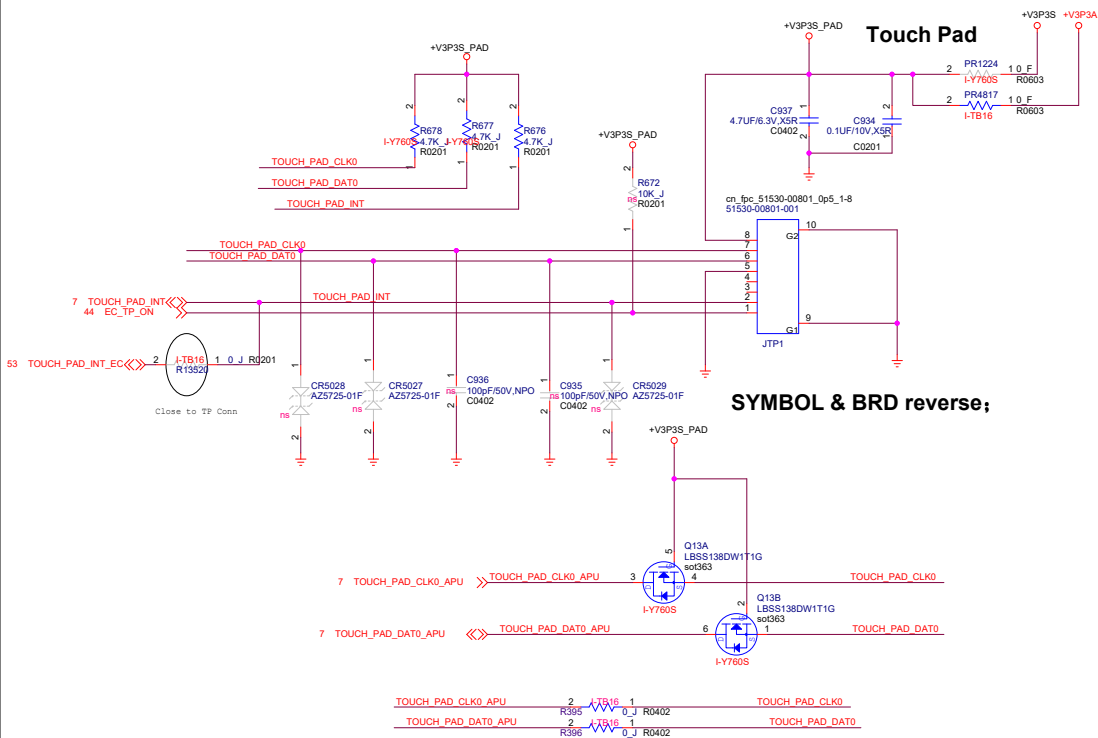
A

A



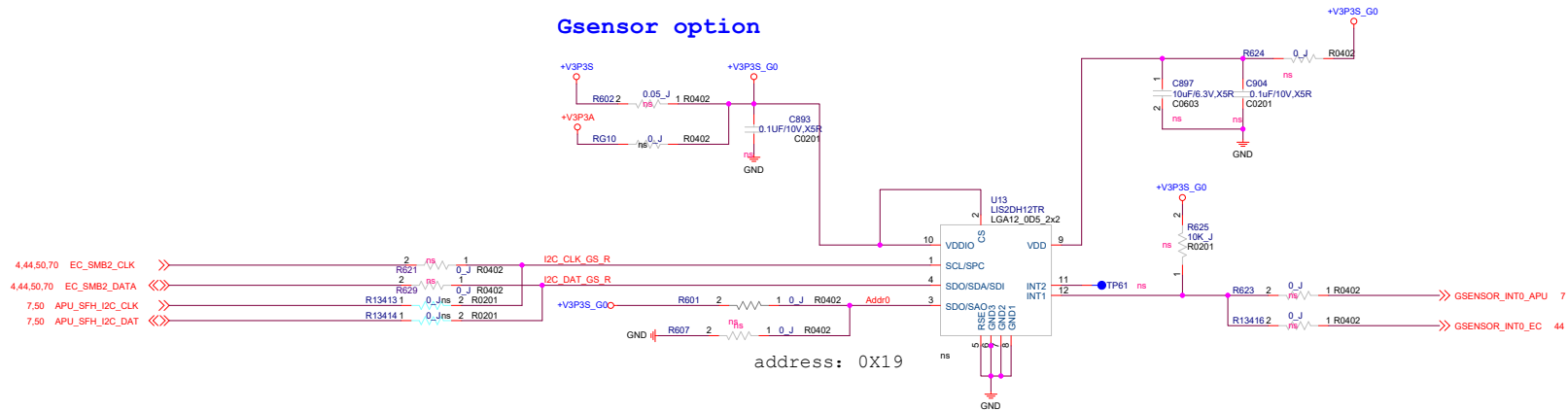




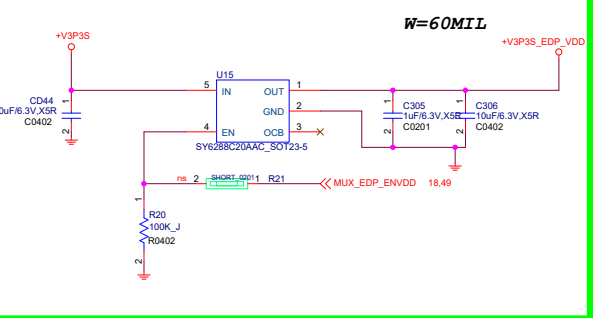


Pin Number	Pin Name	Description
1	VDD	Power
2	I2C-CLK	I2C_Clock
3	I2C-DAT	I2C_Data
4	GN	Ground
5	N/C	N/C
6	N/C	N/C
7	ATTN	Attention/Interrupt (Active Low, Open Drain)
8	LID CLOSE	Input for LID Close event/Disable Touch Pad (Active Low)

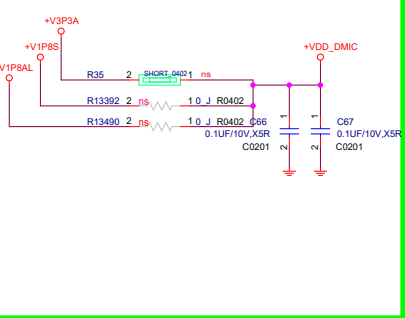
Gsensor option



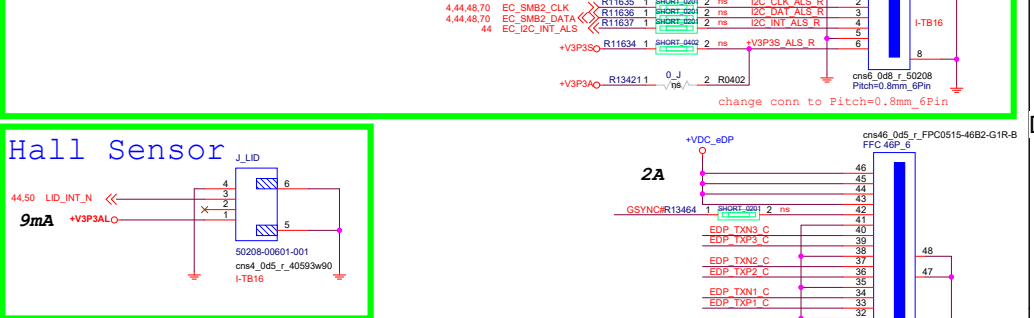
EDP Logic Power



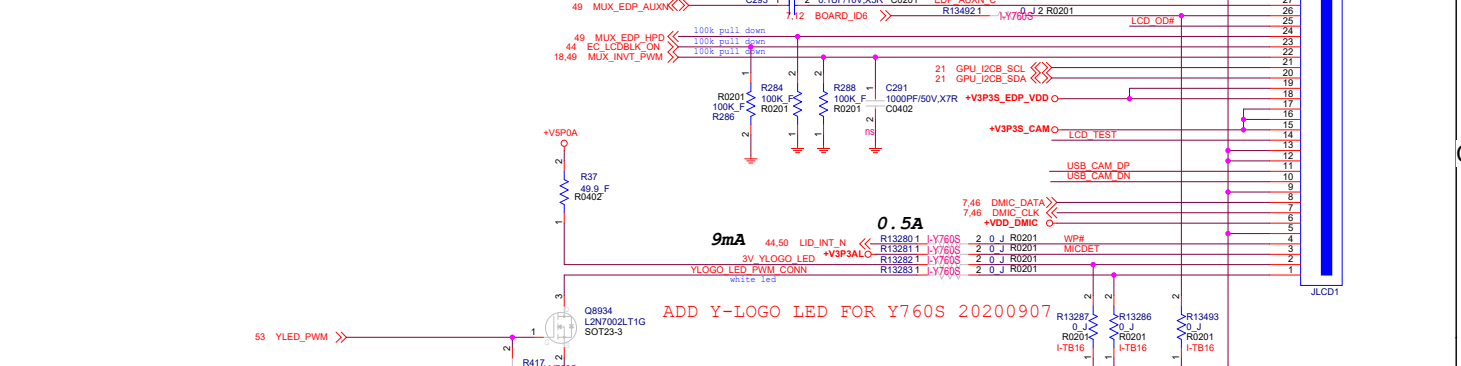
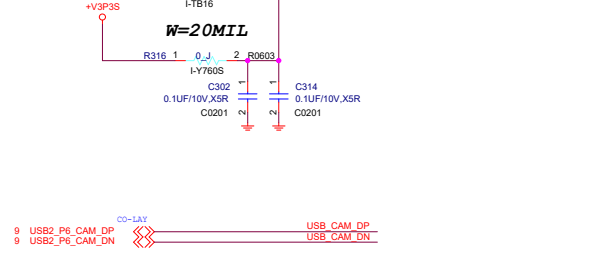
DMIC Power



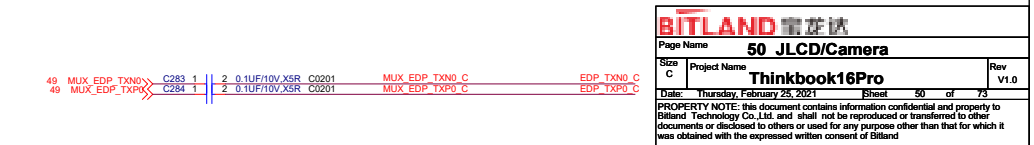
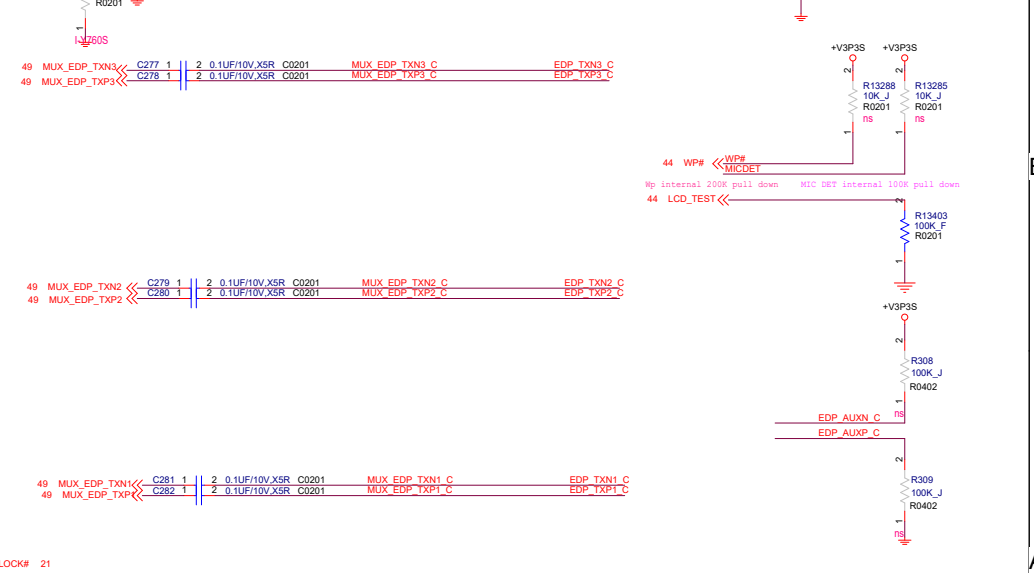
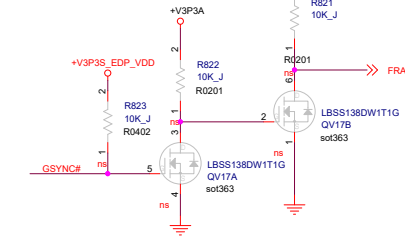
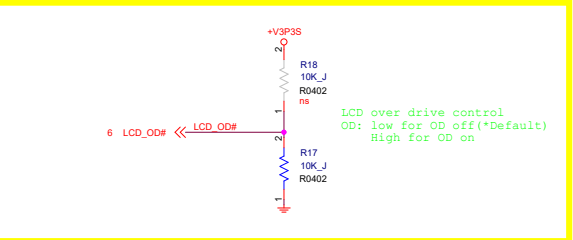
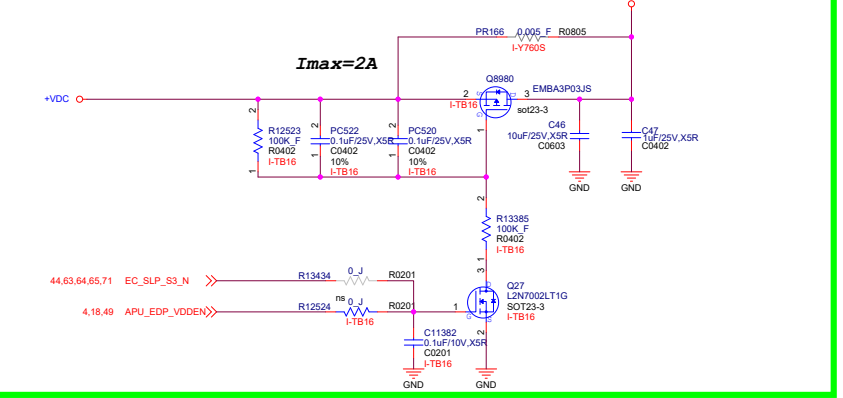
ALS

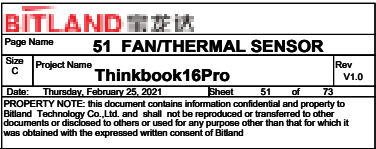


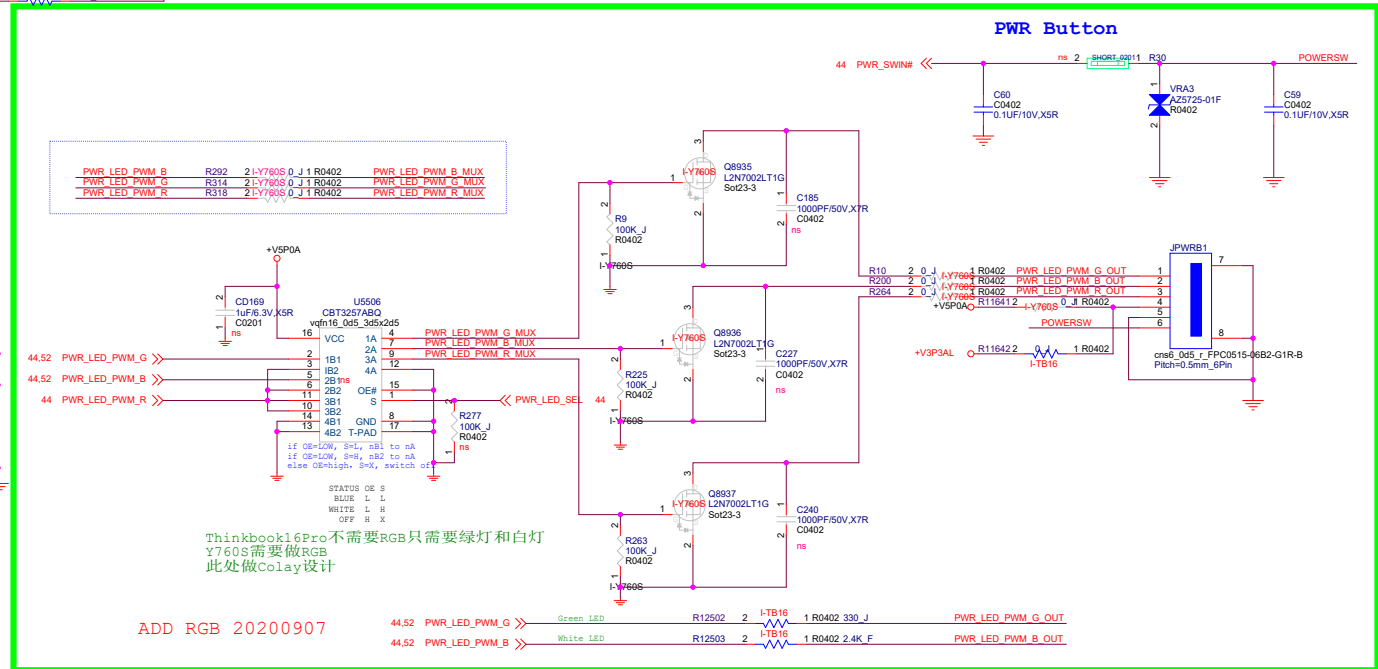
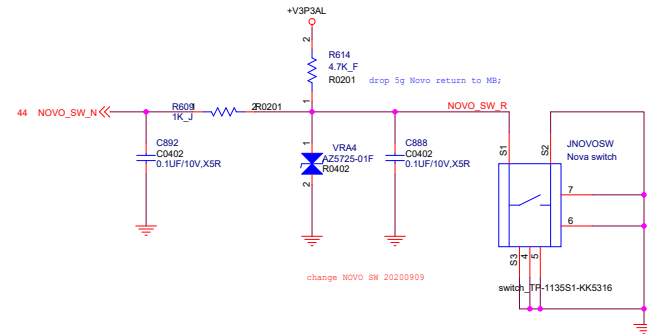
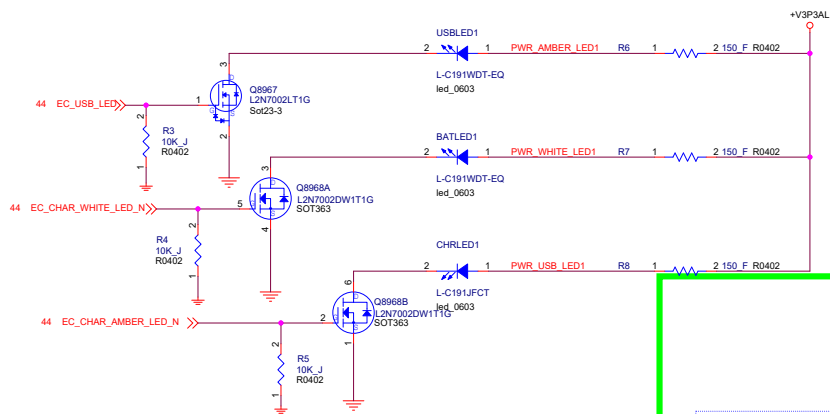
Camera



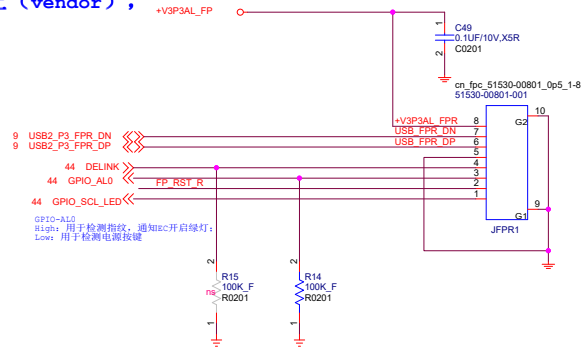
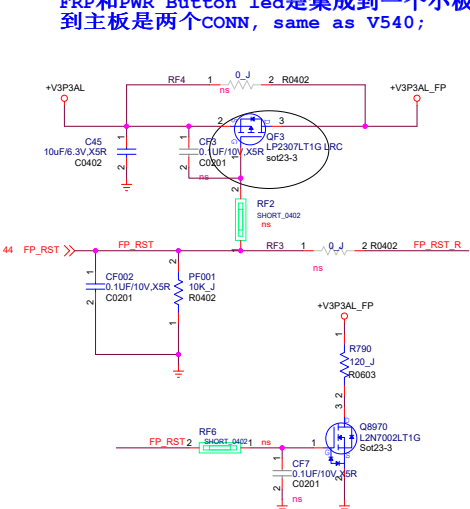
LCD Backlight Power



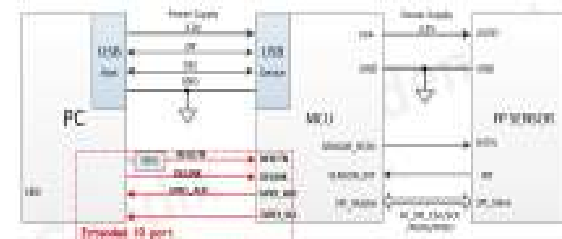




FRP和PWR Button led是集成到一个小板上 (vendor)，到主板是两个CONN, same as V540;



NO.	PIN NAME	PIN DEFINE
1	LED	LED控制信号
2	RESETN	MCU 复位信号
3	GPIO_AL0	电源屏蔽
4	DELINK	电源状态指示
5	GND	信号地
6	DP	USB信号DP
7	DM	USB信号DM
8	D3V3	3.3V电源



PC和MCU的连接图，显示了USB2_P3_FPR_DN和USB2_P3_FPR_DP的连接。

Page Name

52 Buttons/PWR LED/FRP/CON

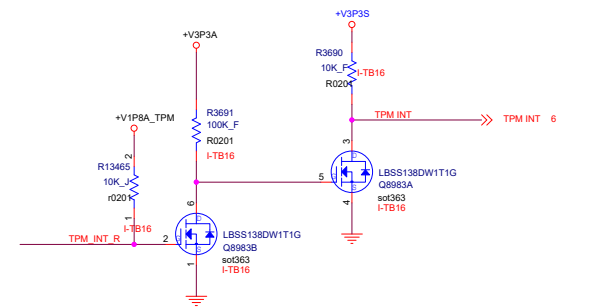
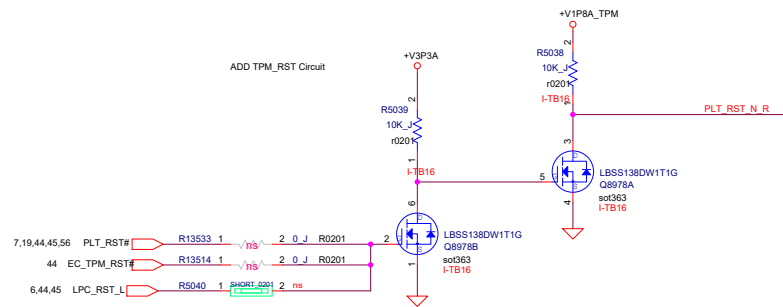
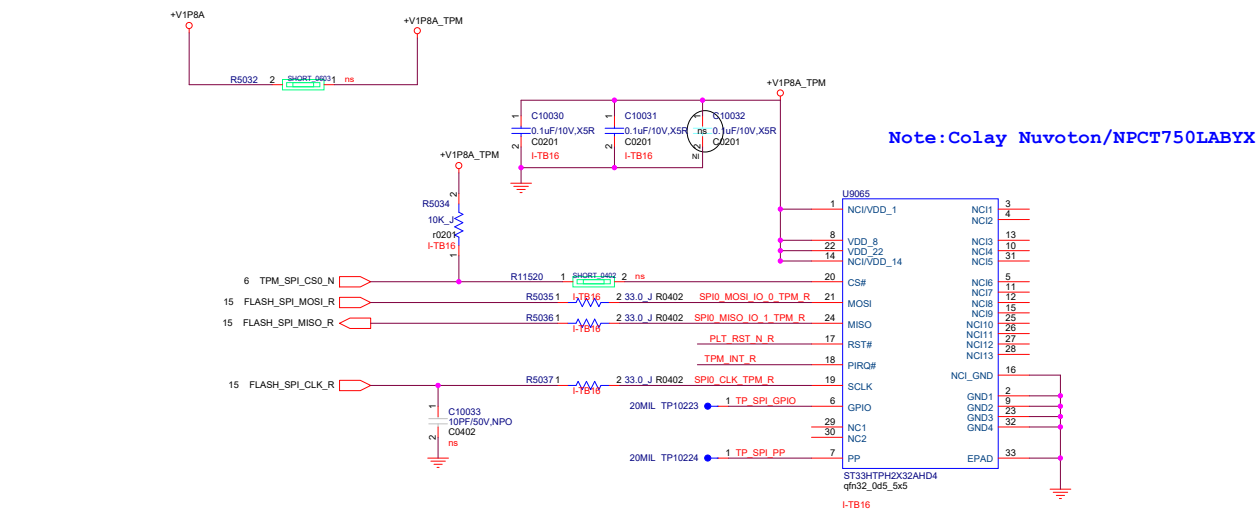
Rev V1.0

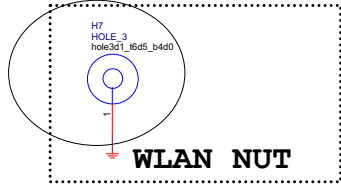
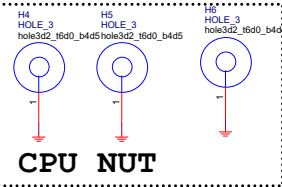
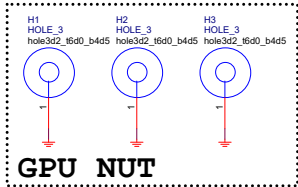
Thinkbook16Pro

Monday, March 01, 2021

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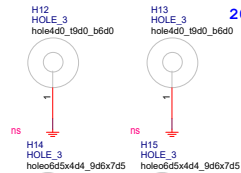
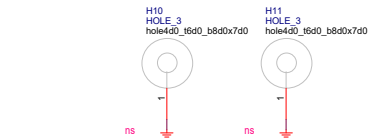
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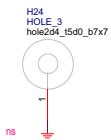
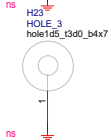
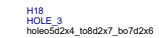
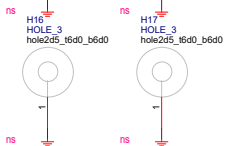
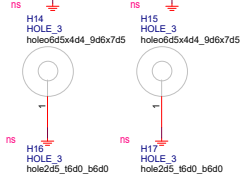


hole3d2_t6d0_b4d5 x6--CPU&GPU
hole3d1_t4d0_b6d5 x1--wlan

hole4d0_t6d0_b8d0x7d0 x3
holeo5d2x4_t6d0x6_bo7d2x6 x1
hole4d0_t9d0_b6d0 x2
hole4d4_c7d5 x2
hole2d5_t6d0_b6d0 x2

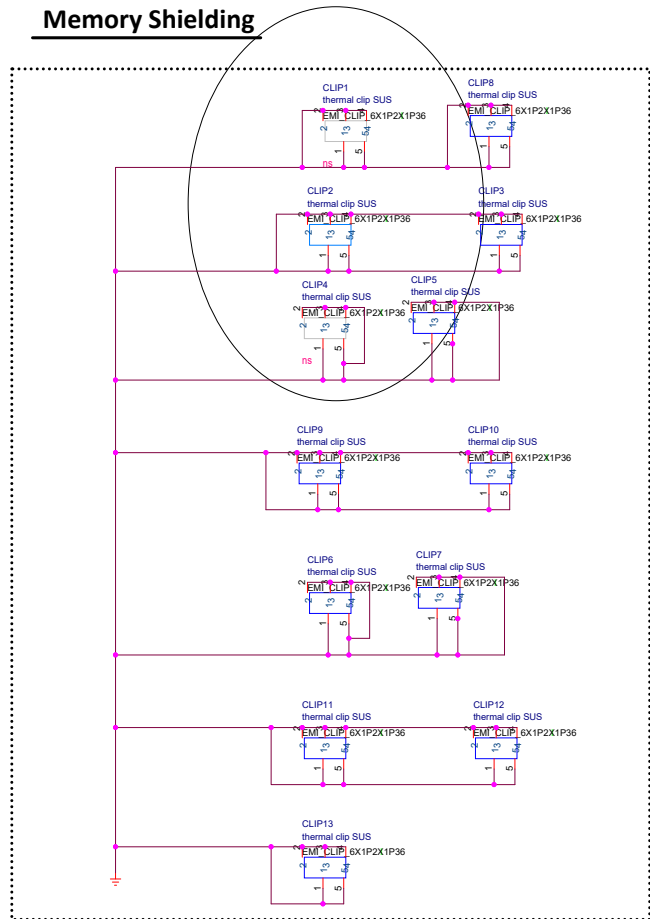


20200923: Delete H9 for Y760S UMA and DIS colay

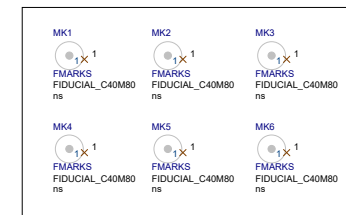


MB HOLE
not install

Memory Shielding




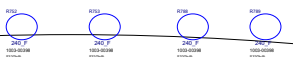



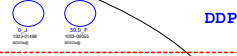








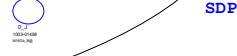






optical dot
top 3pcs
bot 3pcs









BITLAND		
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Size C	Project Name Thinkbook16Pro	Rev V1.0
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DRAM and RES

DRAM PN	BOARD ID	CONFIGURE	UZQ E9 Pin	T7 Pin	SDP/DDP M9 Pin
		Samsung 16Gb		NC	
		Samsung 32Gb			DDP
		Micron 16Gb MT40A1G16RD-062E:E		NC	
		Micron 32Gb		NC	
		SK Hynix 16Gb H5ANAG6NCR-XNC			DDP
		SK Hynix 32Gb			DDP
		Micron 16Gb MT40A1G16RC-062E:B		NC	
		Hynix 16Gb MT40A1G16RC-062E:B		NC	



VRAM and RES

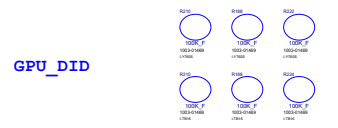
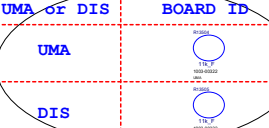

VRAM CONFIGURE	BOARD ID	VRAM PN
SAMSUNG		
SK Hynix		
MICRON		

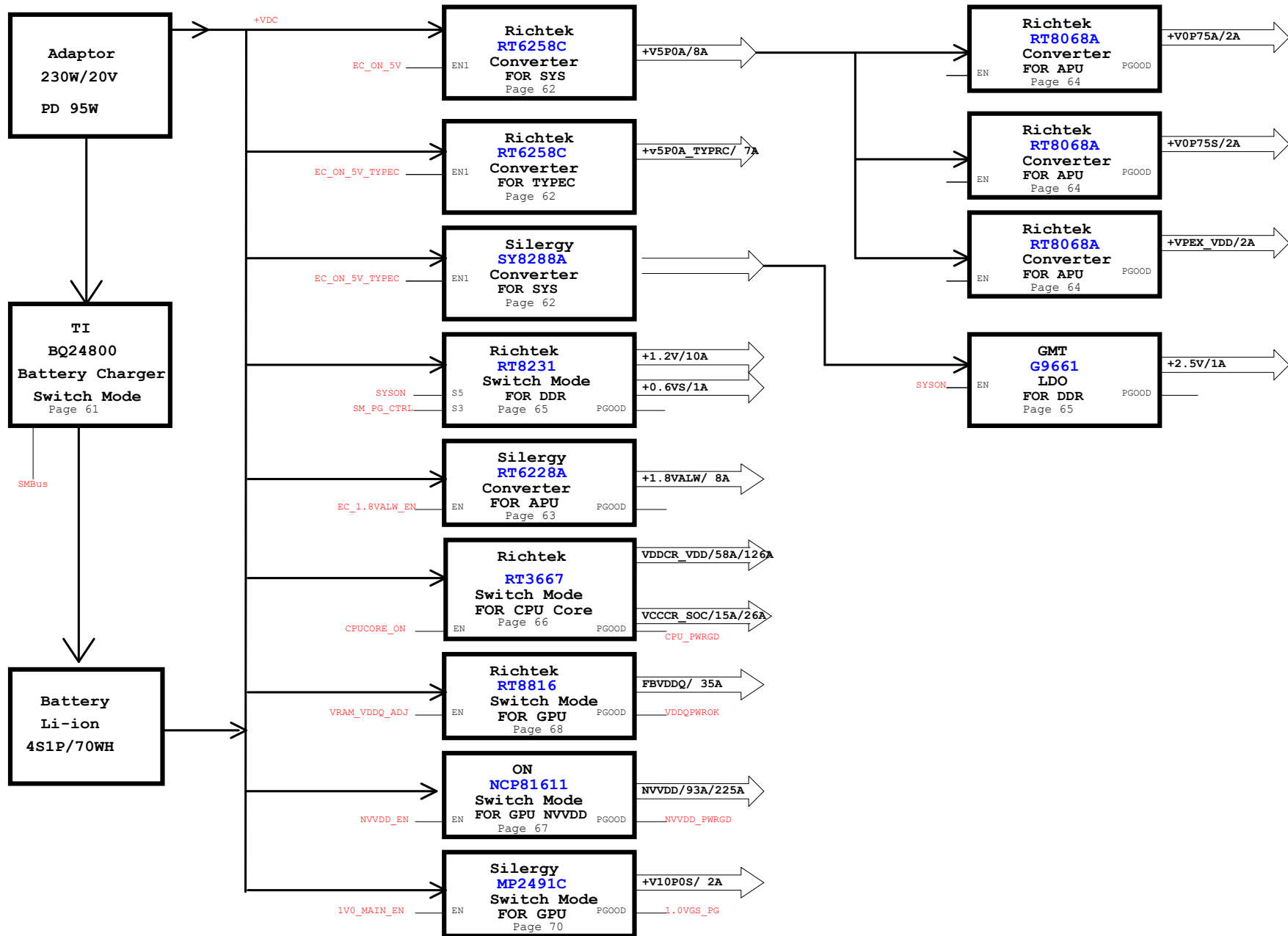
APU PN


MB PN

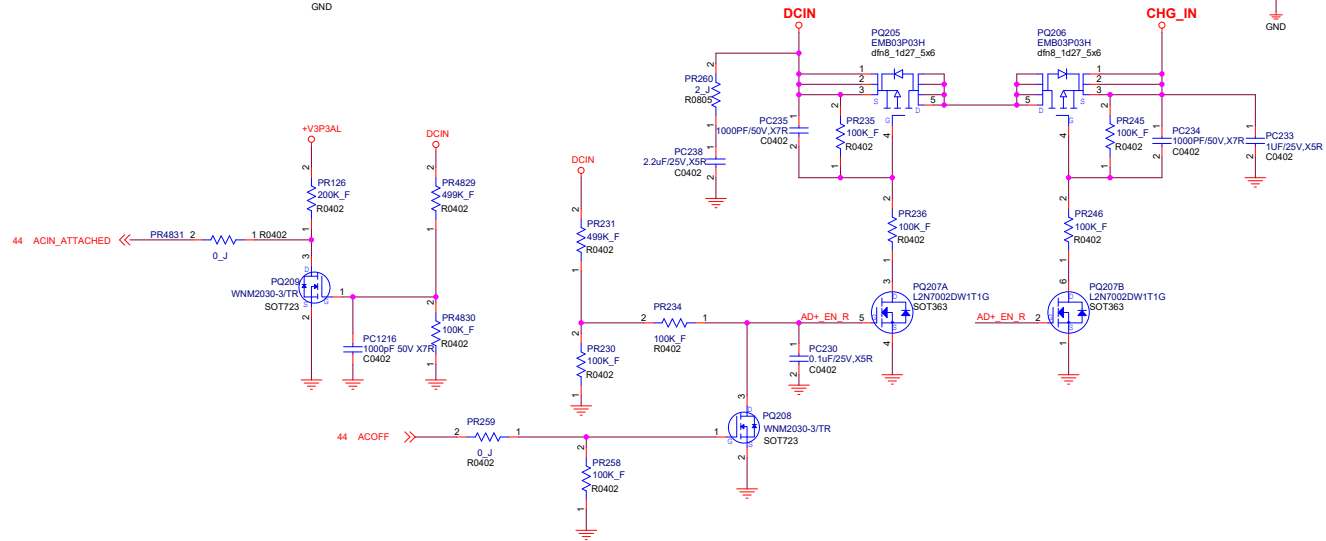
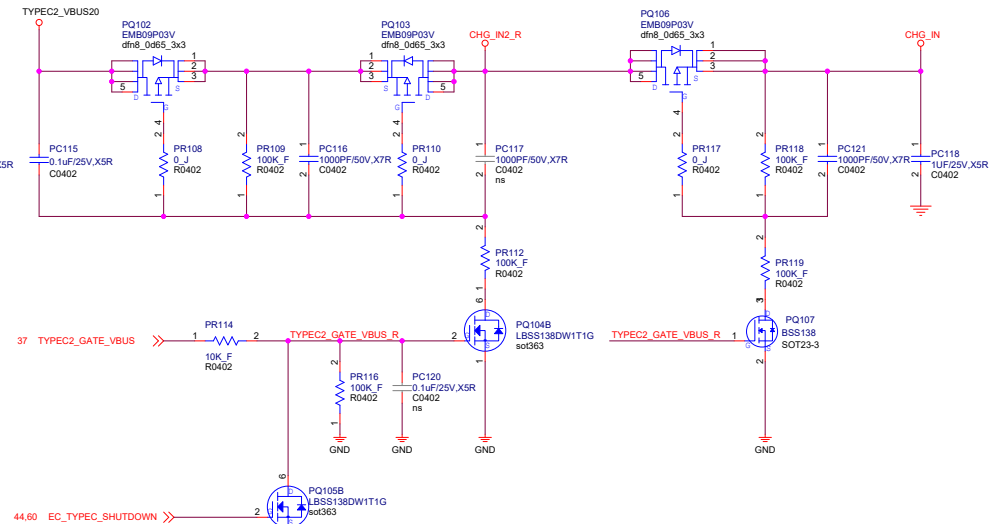
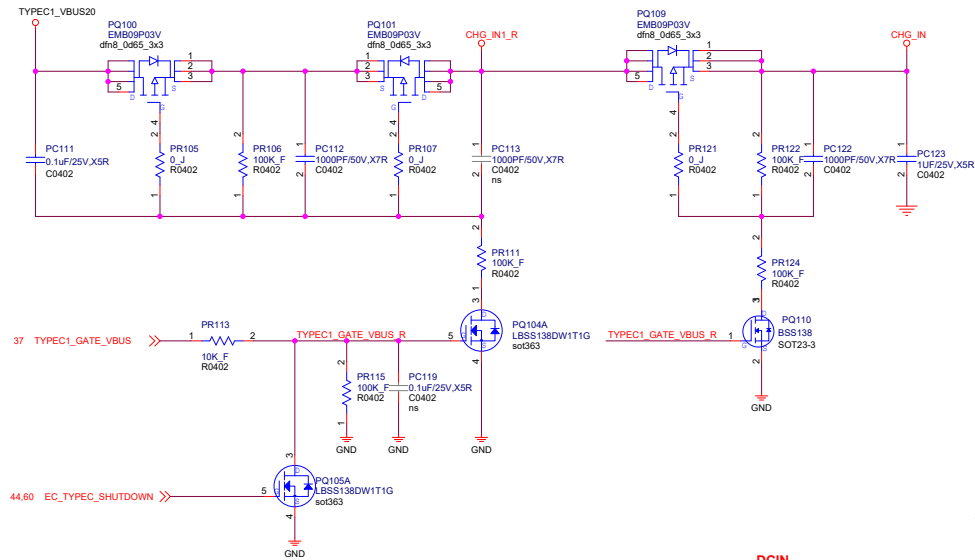
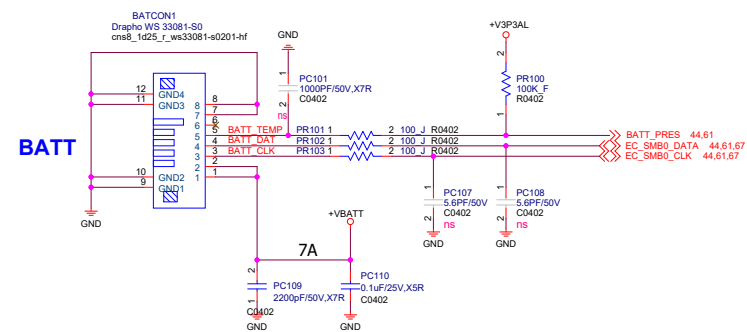
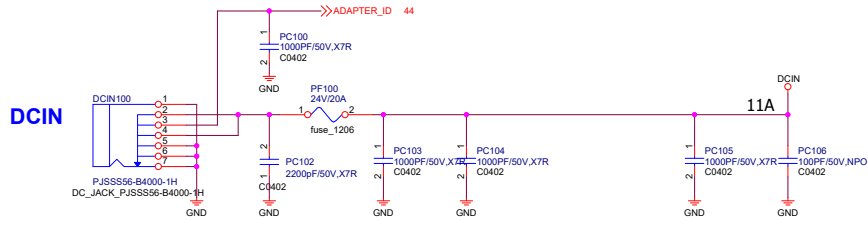

DIS or UMA

GPU CONFIGURE	BOARD ID
E3	
P1-B	

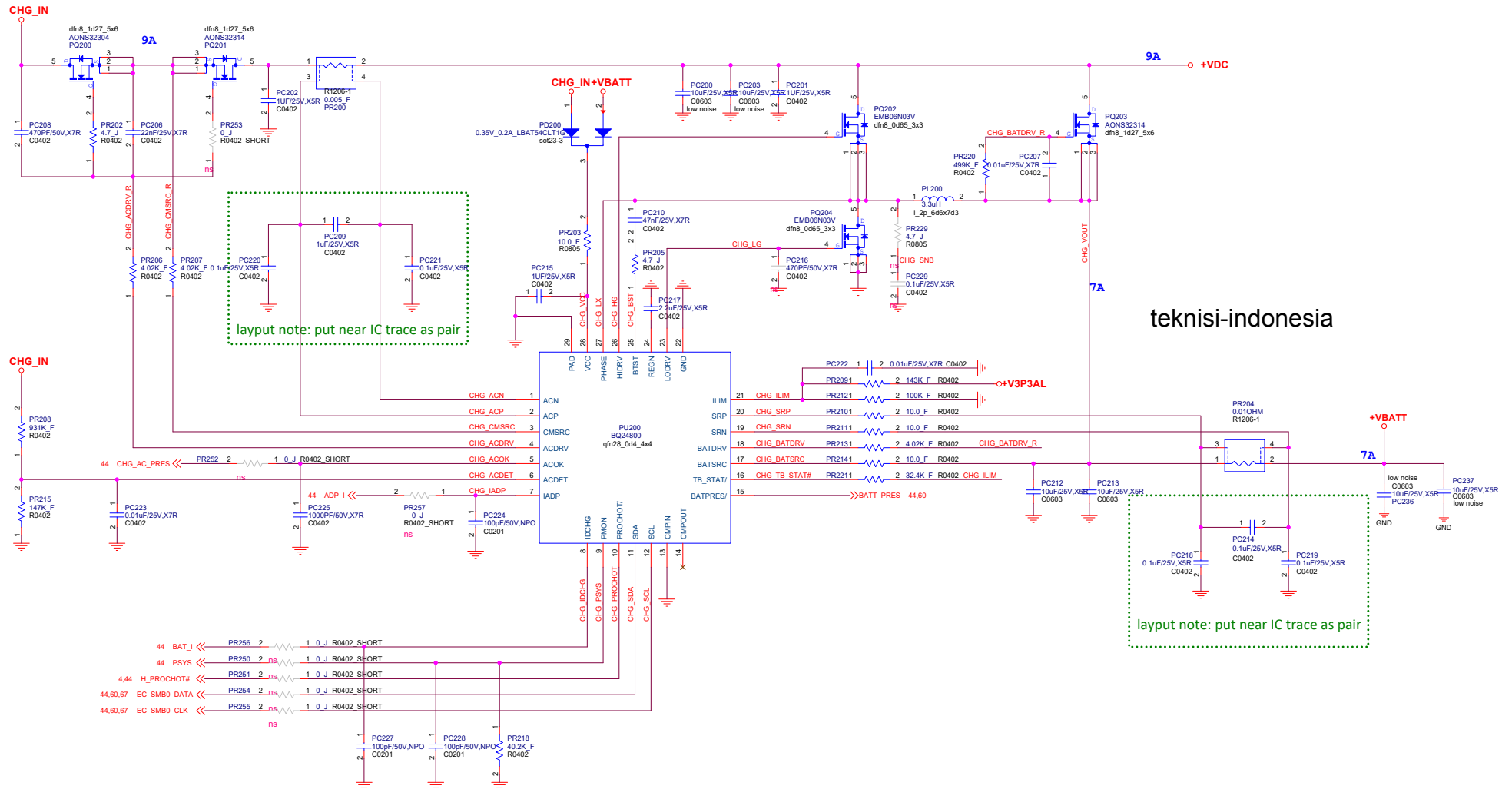
GPU DID	UMA or DIS	BOARD ID
	UMA	
	DIS	

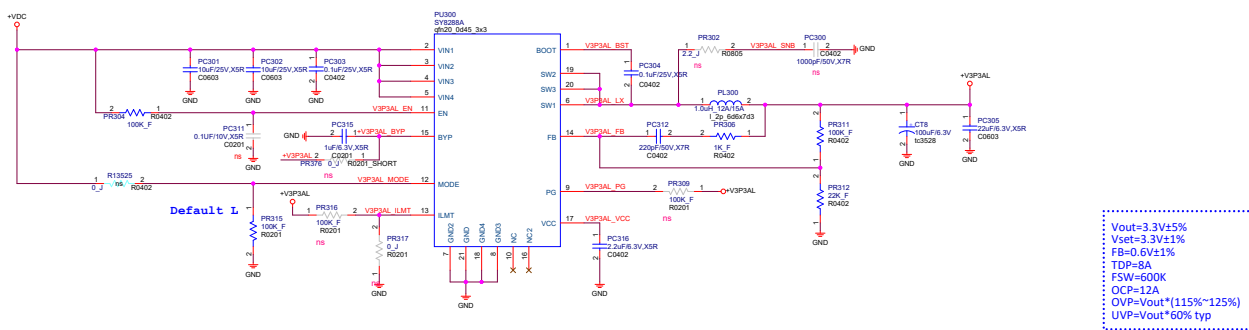
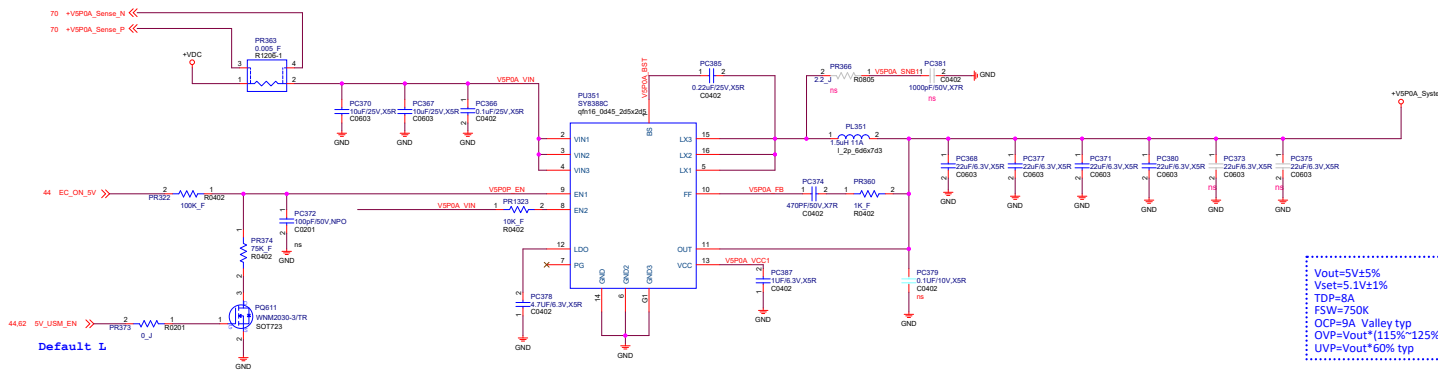
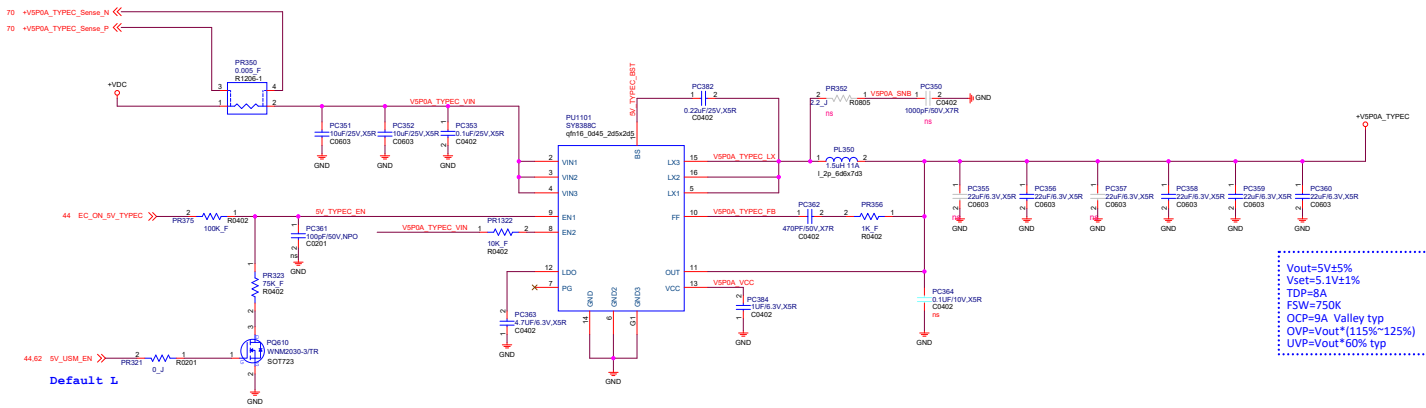


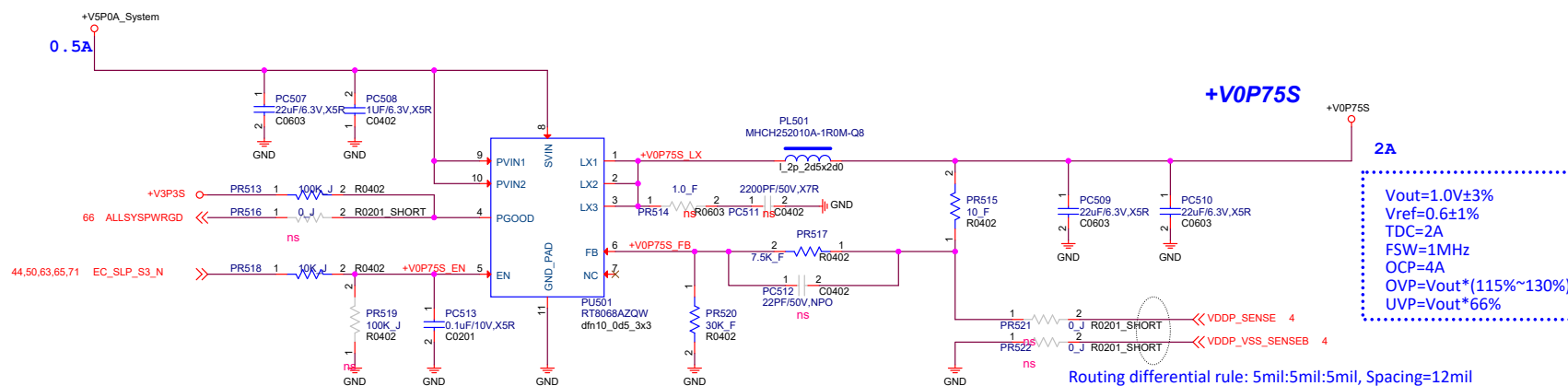
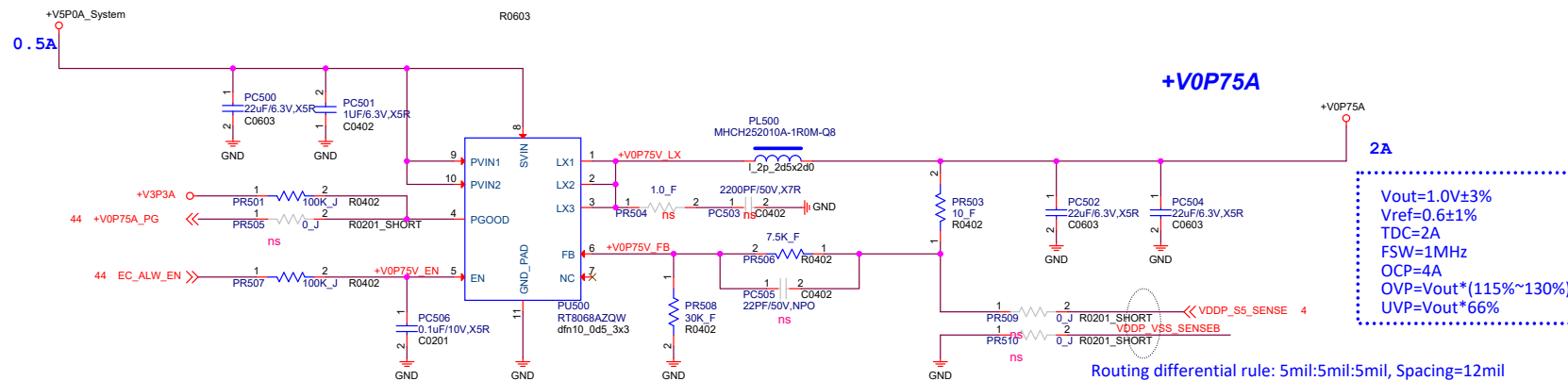
DCIN/BATTERY CONNECTOR



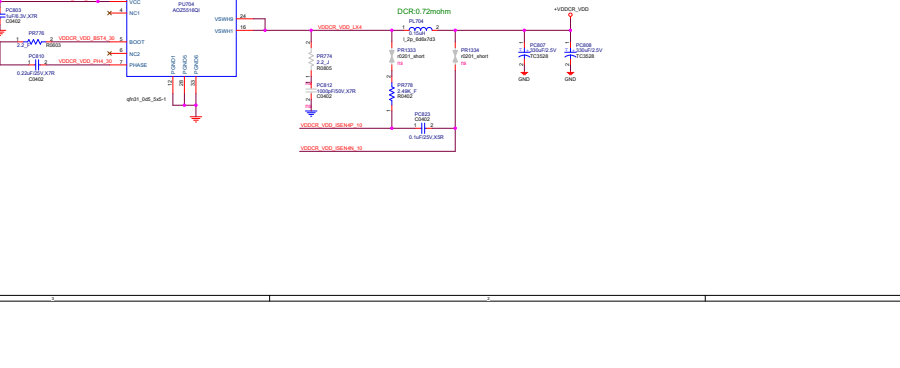
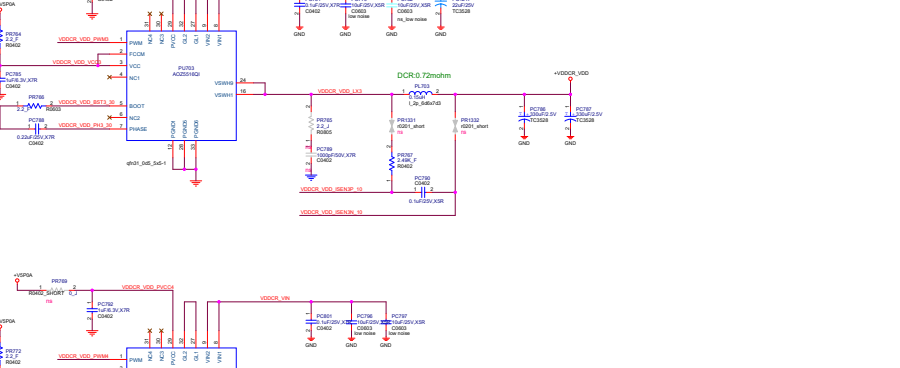
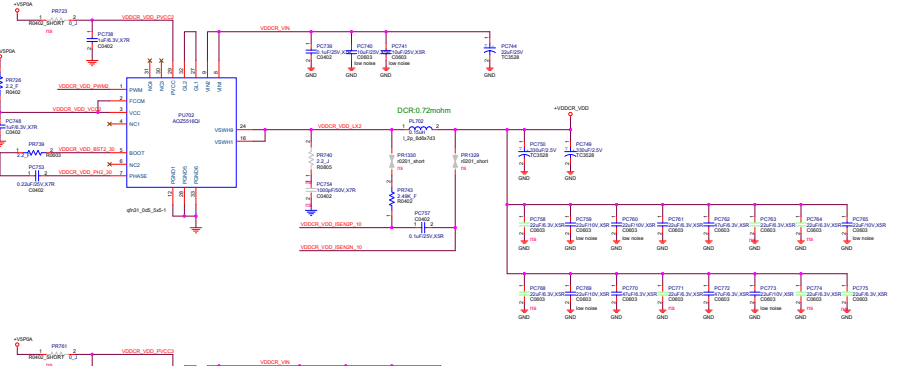
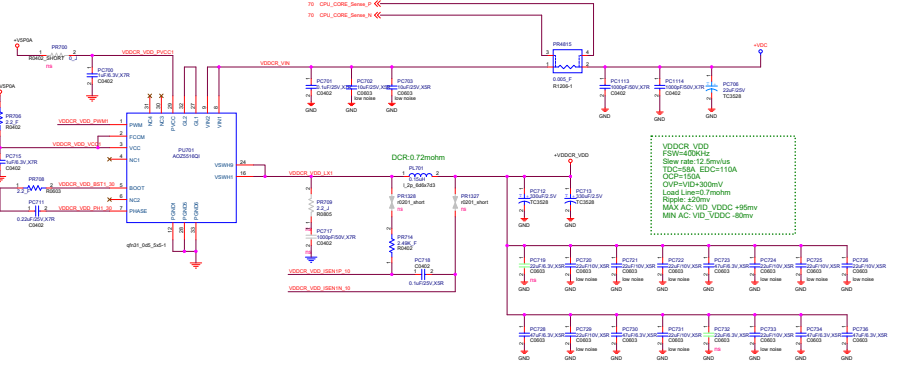
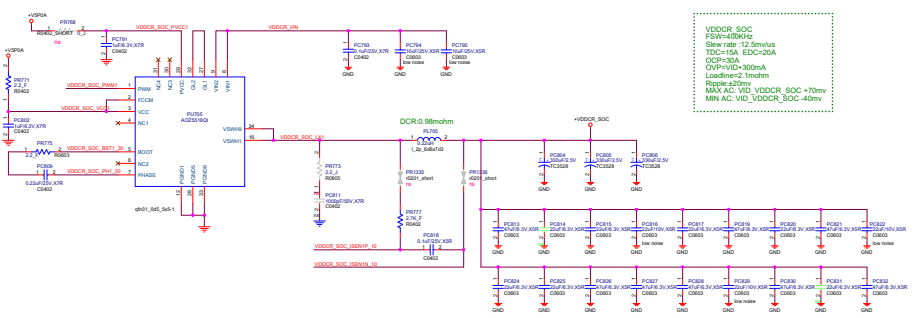
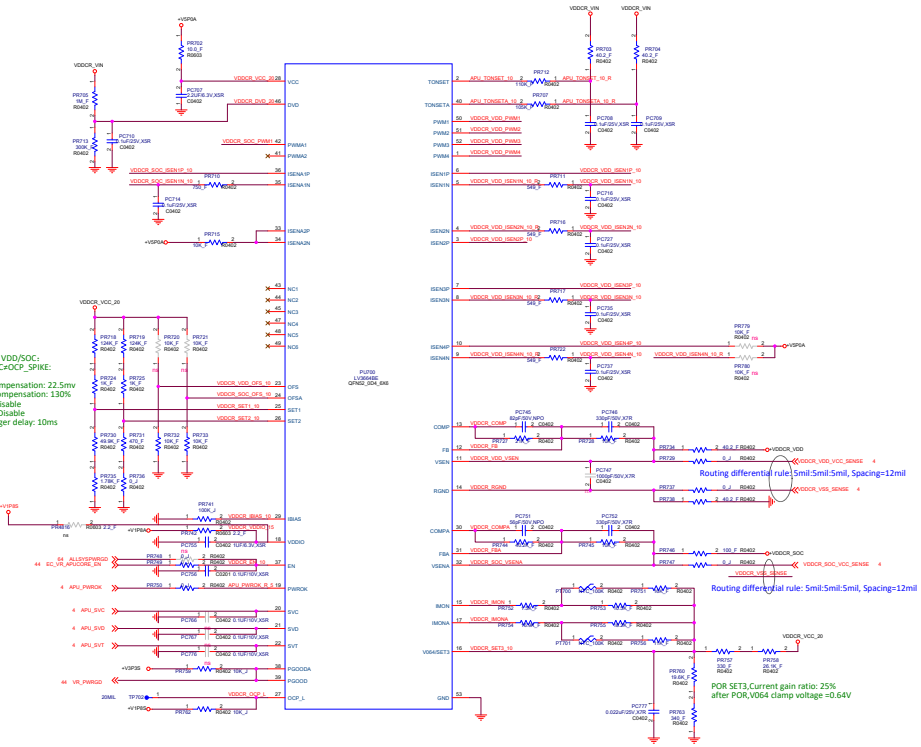
BATTERY CHARGER



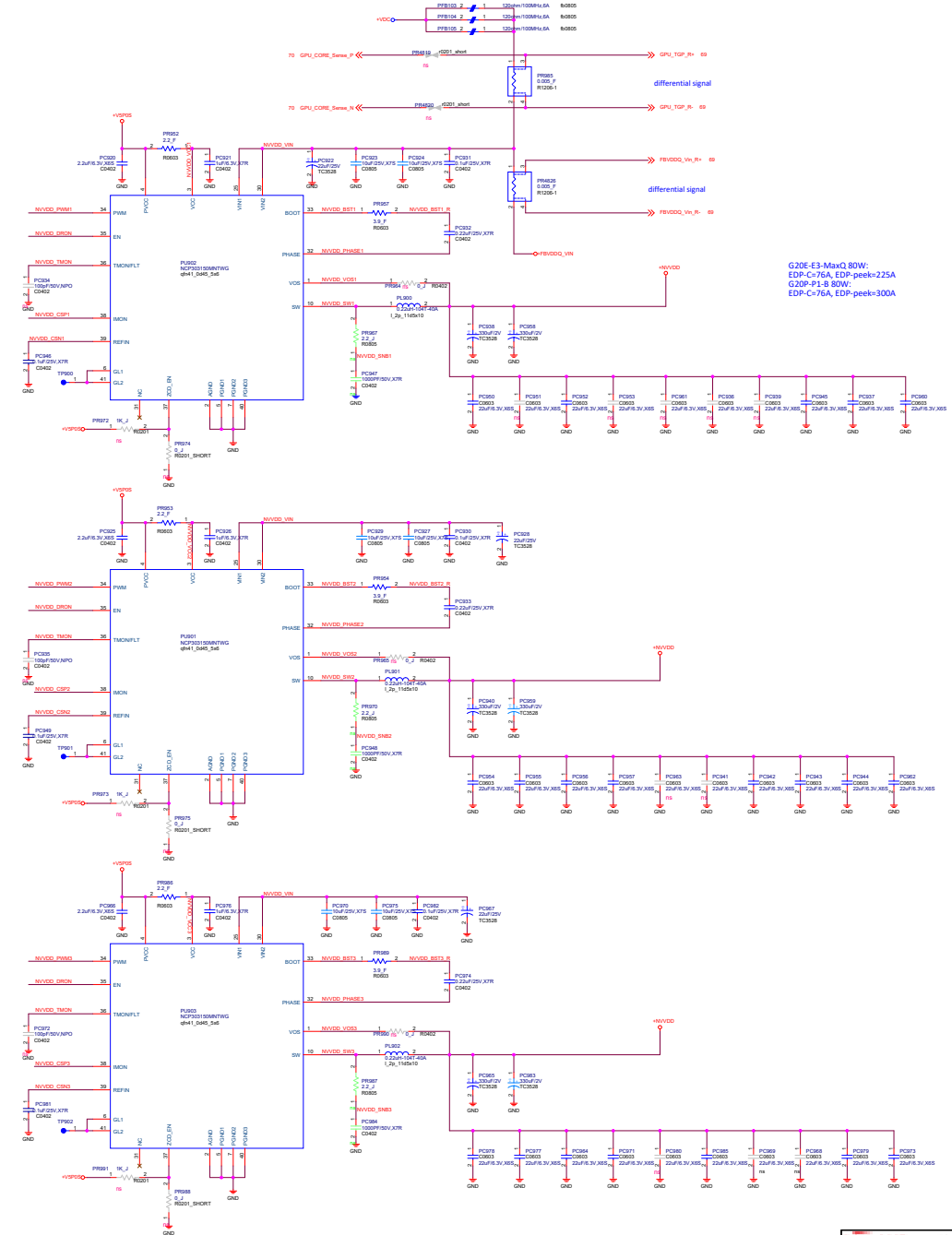
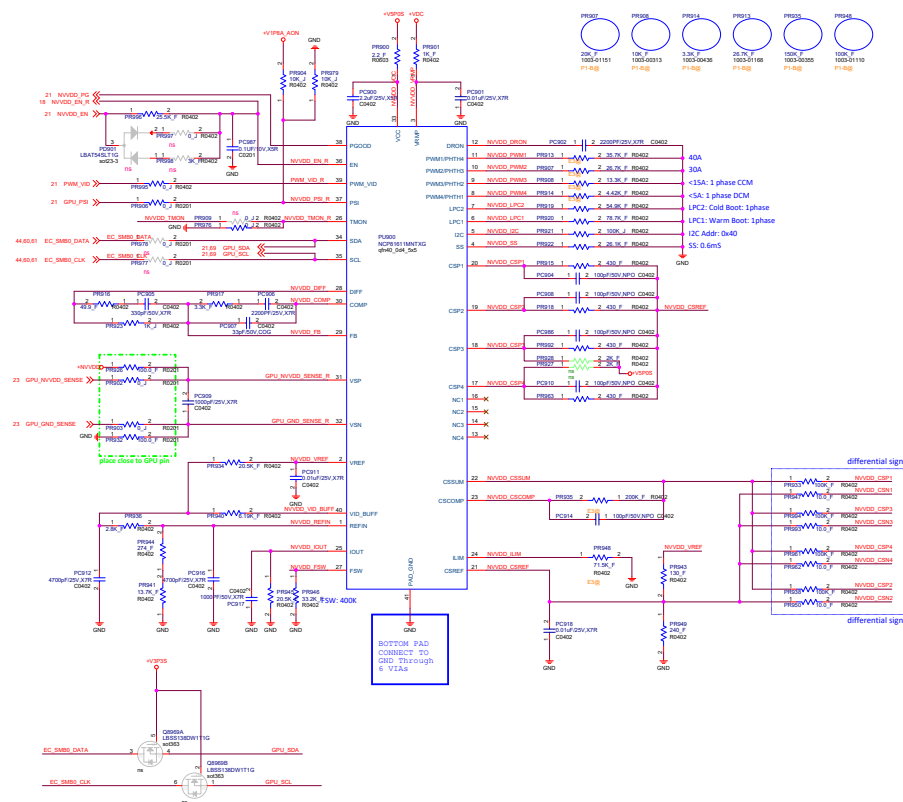




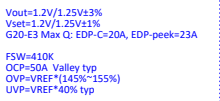
POR SET VDD/SOC:
 OCP_TDC+OCP_SPIKE
 Disable
 DVID Compensation: 22.5mv
 Ramp Compensation: 130%
 ORTH: Disable
 Offset: Disable
 OCP trigger delay: 10ms

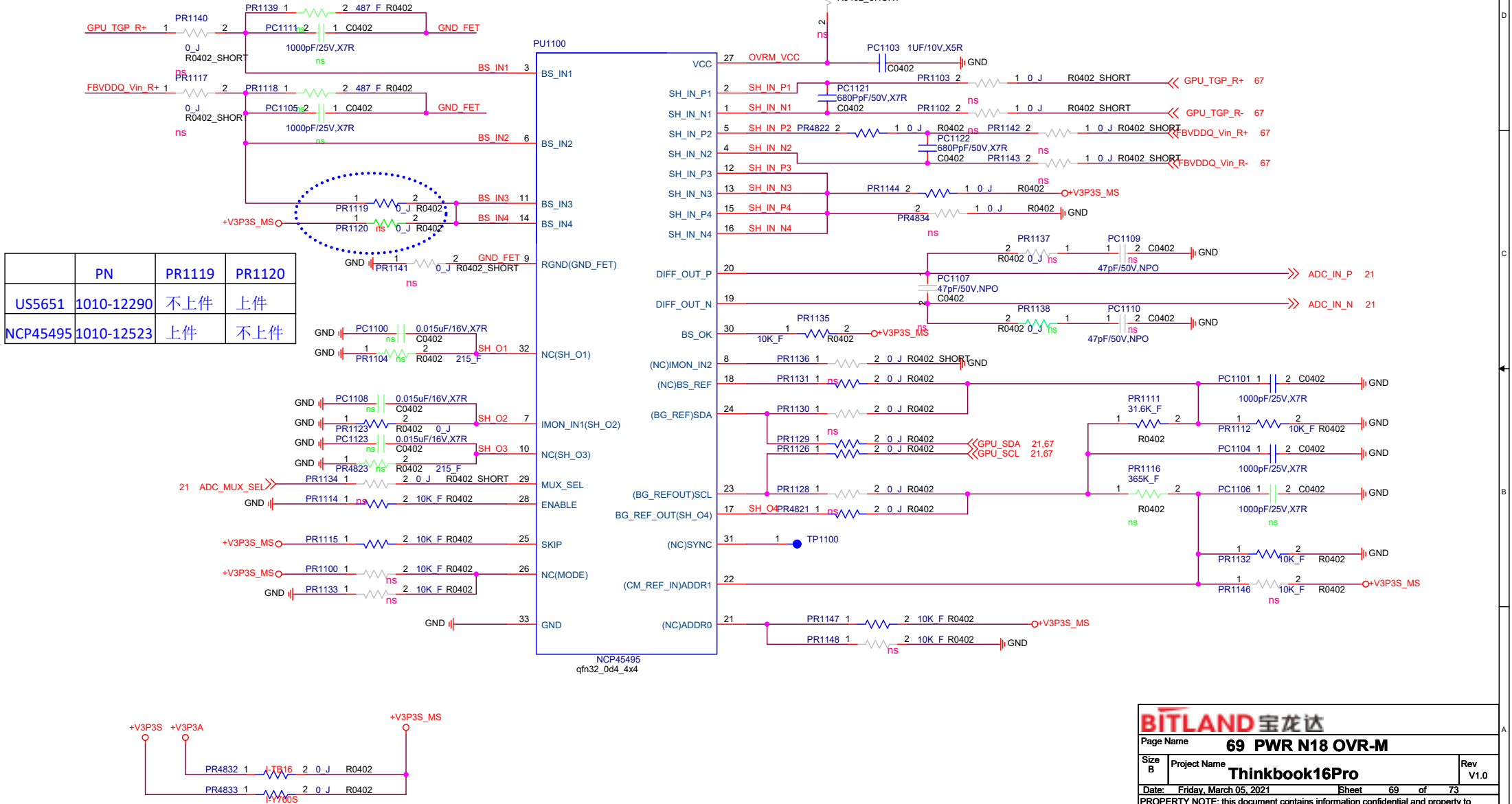


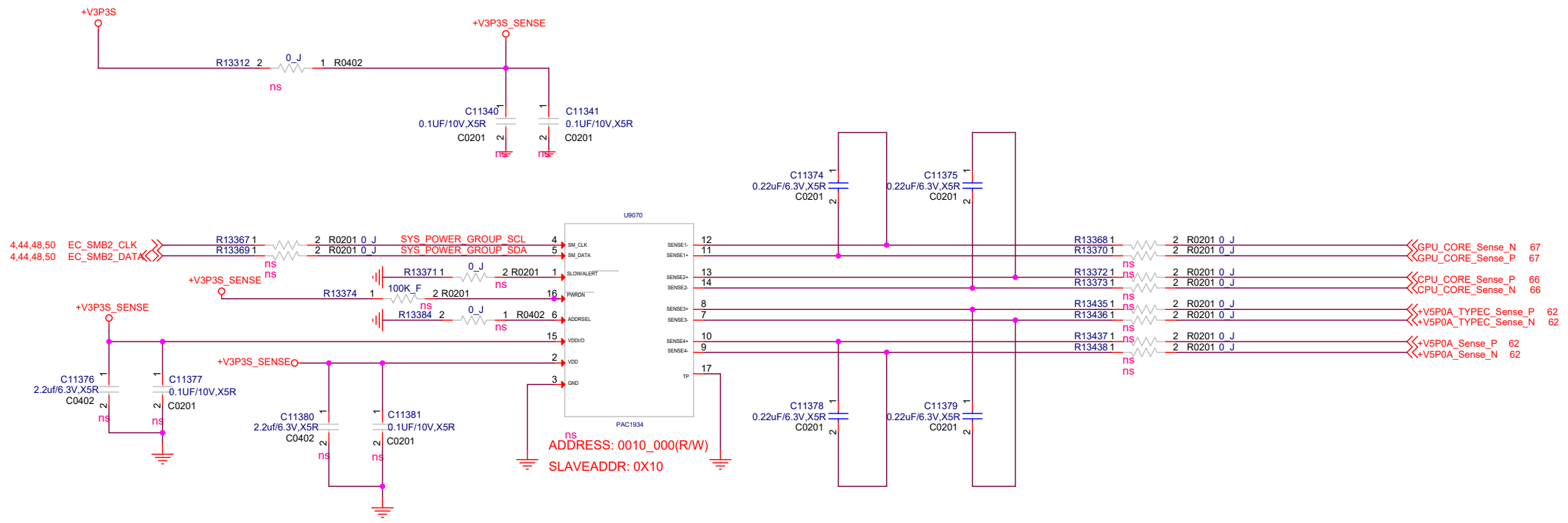
GPU Core power



GPU VRAM POWER

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Page Name

70 PWR CPU&GPU Current Sensor

Size B

Project Name

Thinkbook16Pro

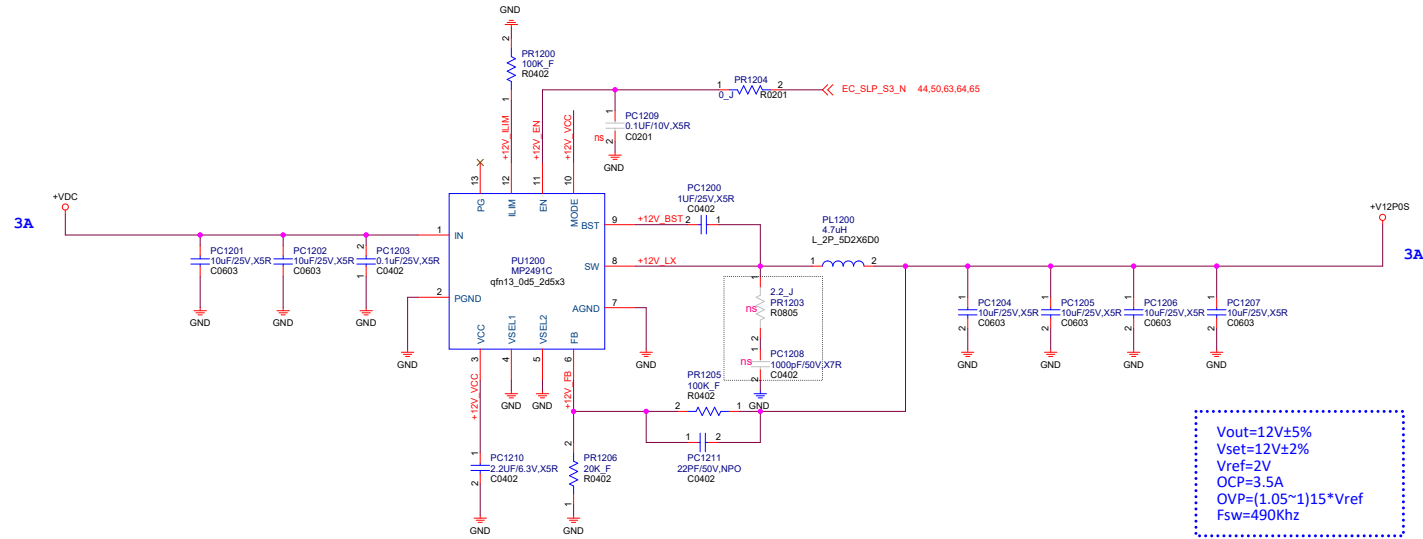
Rev V1.0

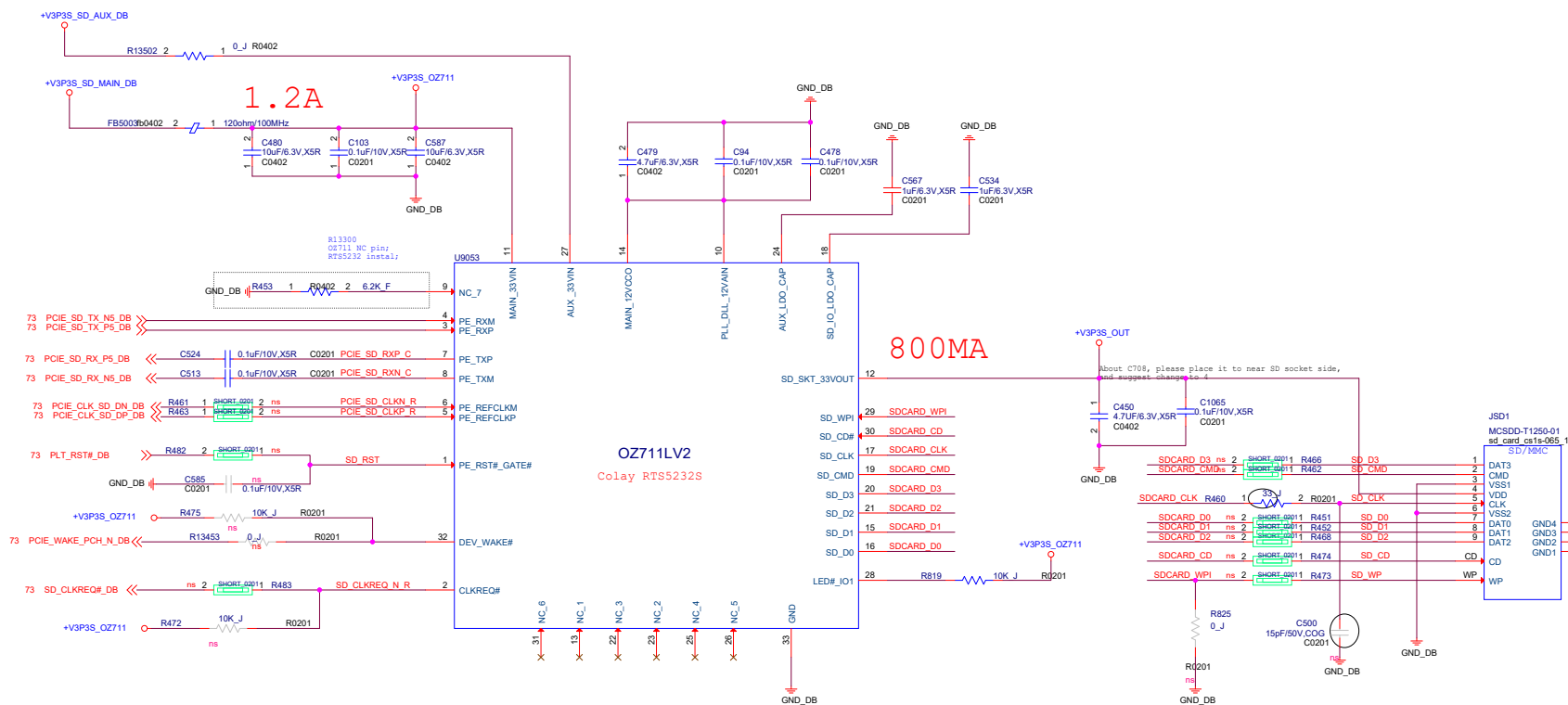
Date: Friday, March 05, 2021

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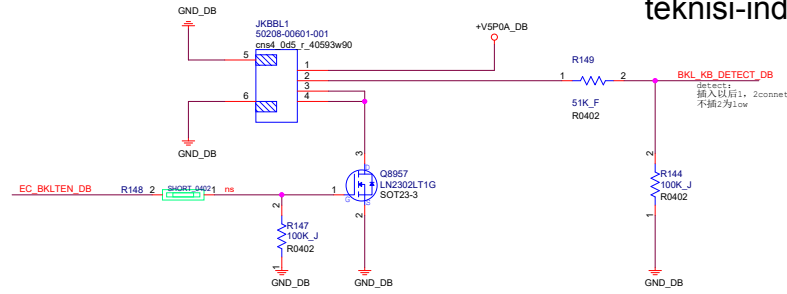
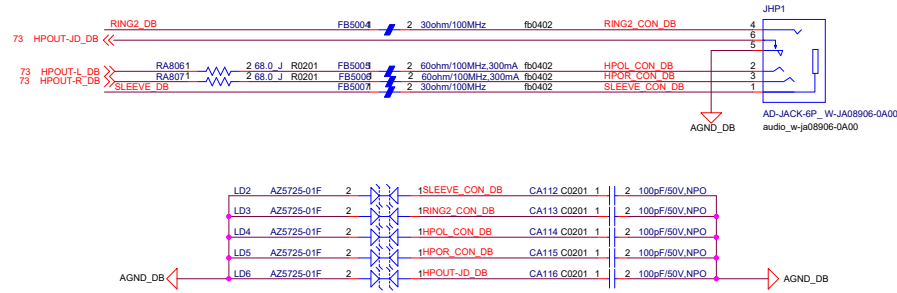
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12V for Fan and SMAMP

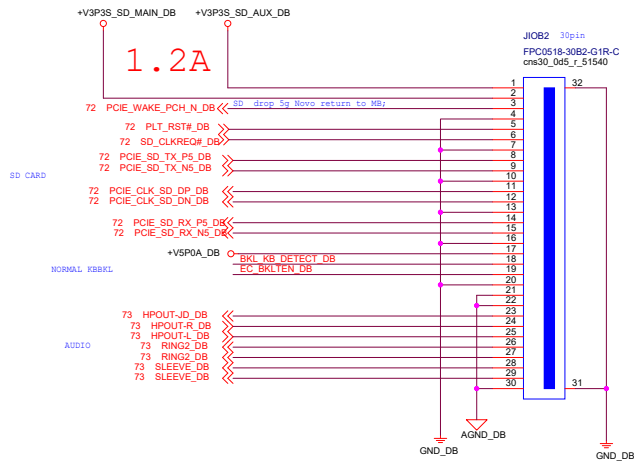
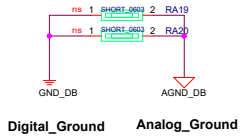




Two MIC-VREF0 design is able to save more power consumption for the headset application.



teknisi-indonesia

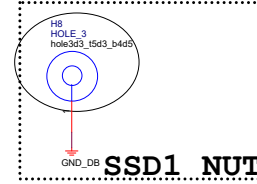


Sub-board

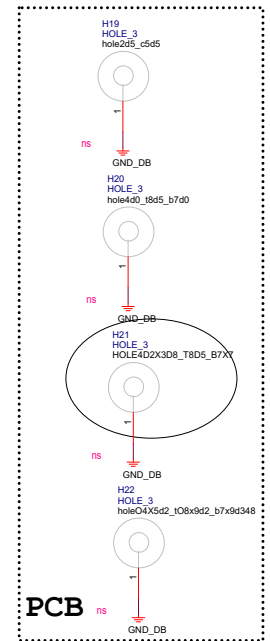
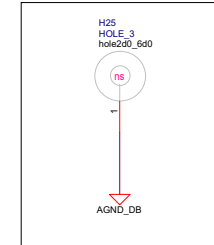
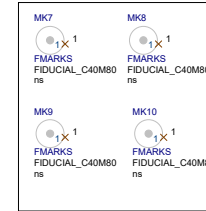
SD CARD DB

AUDIO

hole3d3_t4d5_b5d3--SSD
hole2d5_c5d5
hole4d0_t8d5_b7d0
hole4d0_t8d5_b7x7
hole04X5d2_t08x9d2_b7x9d348



optical dot
top 2pcs
bot 2pcs



BITLAND			
Page Name 73 Sub board(IO BOARD)			
Size C	Project Name	Rev	
	Thinkbook16Pro	V1.0	
Date:	Thursday, February 28, 2021	Sheet	Y3 of Y3
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